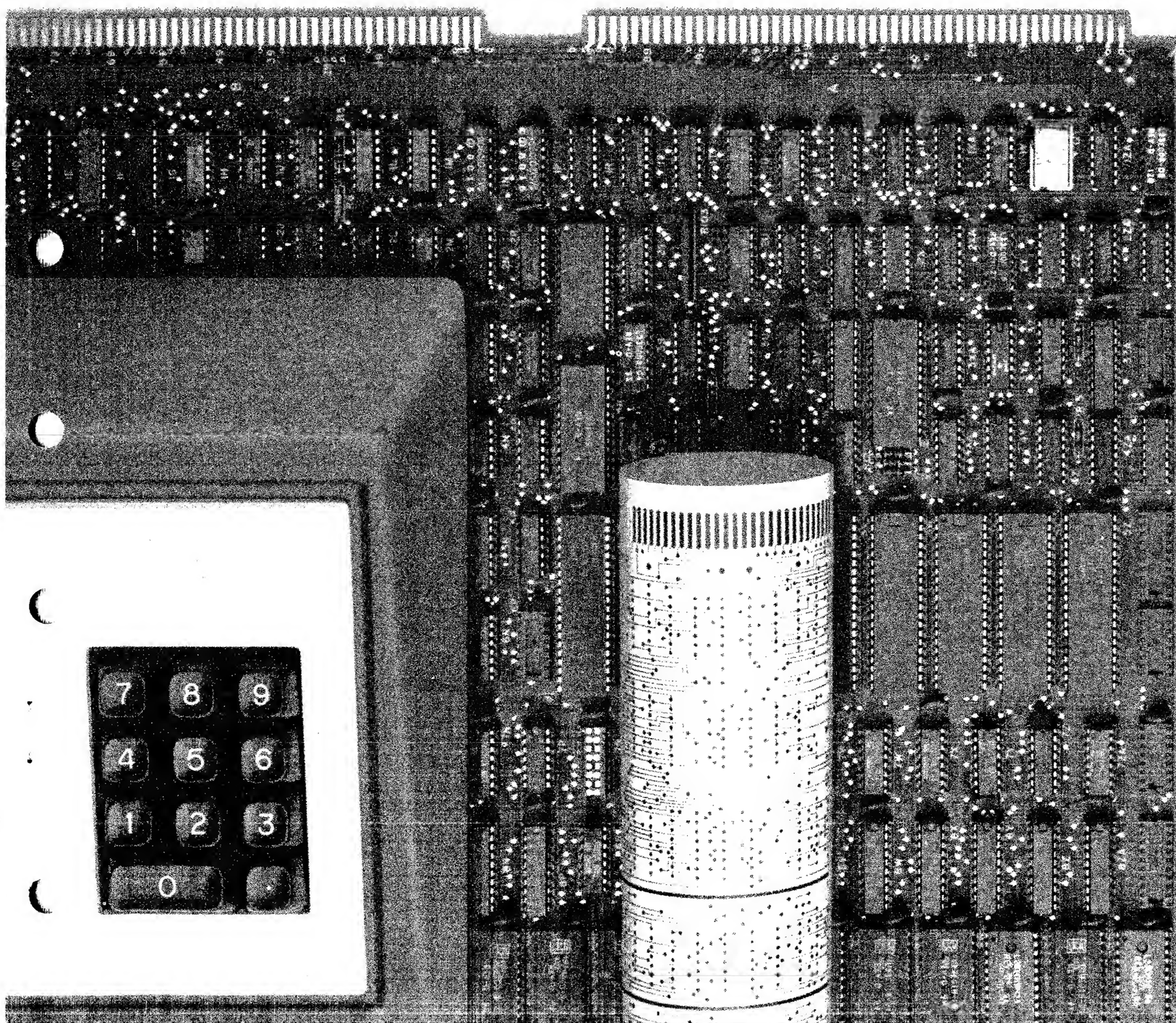
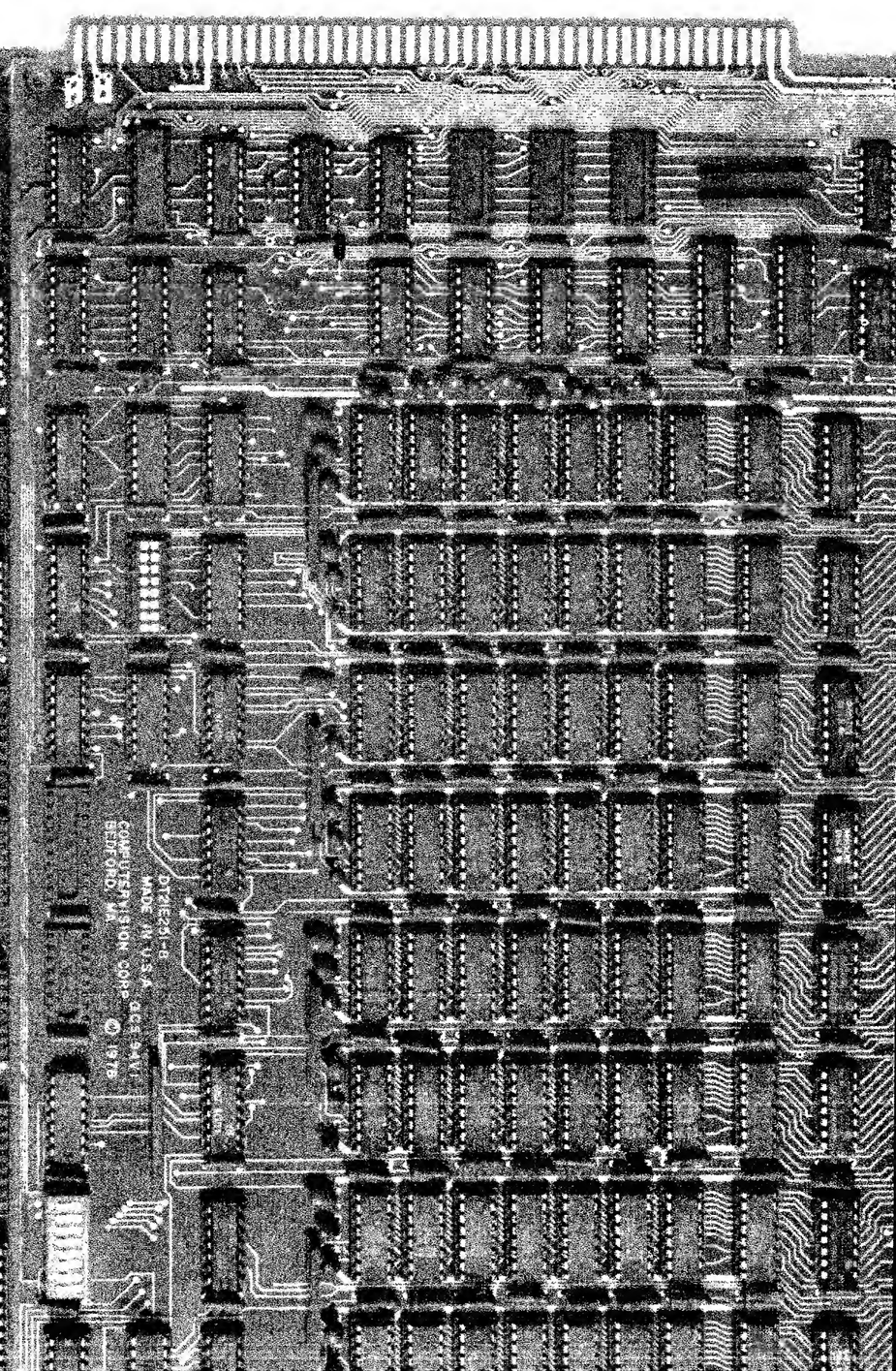
COMPUTERVISION

Technical

Programmable Communications Unit (PCU)

Logic Diagrams



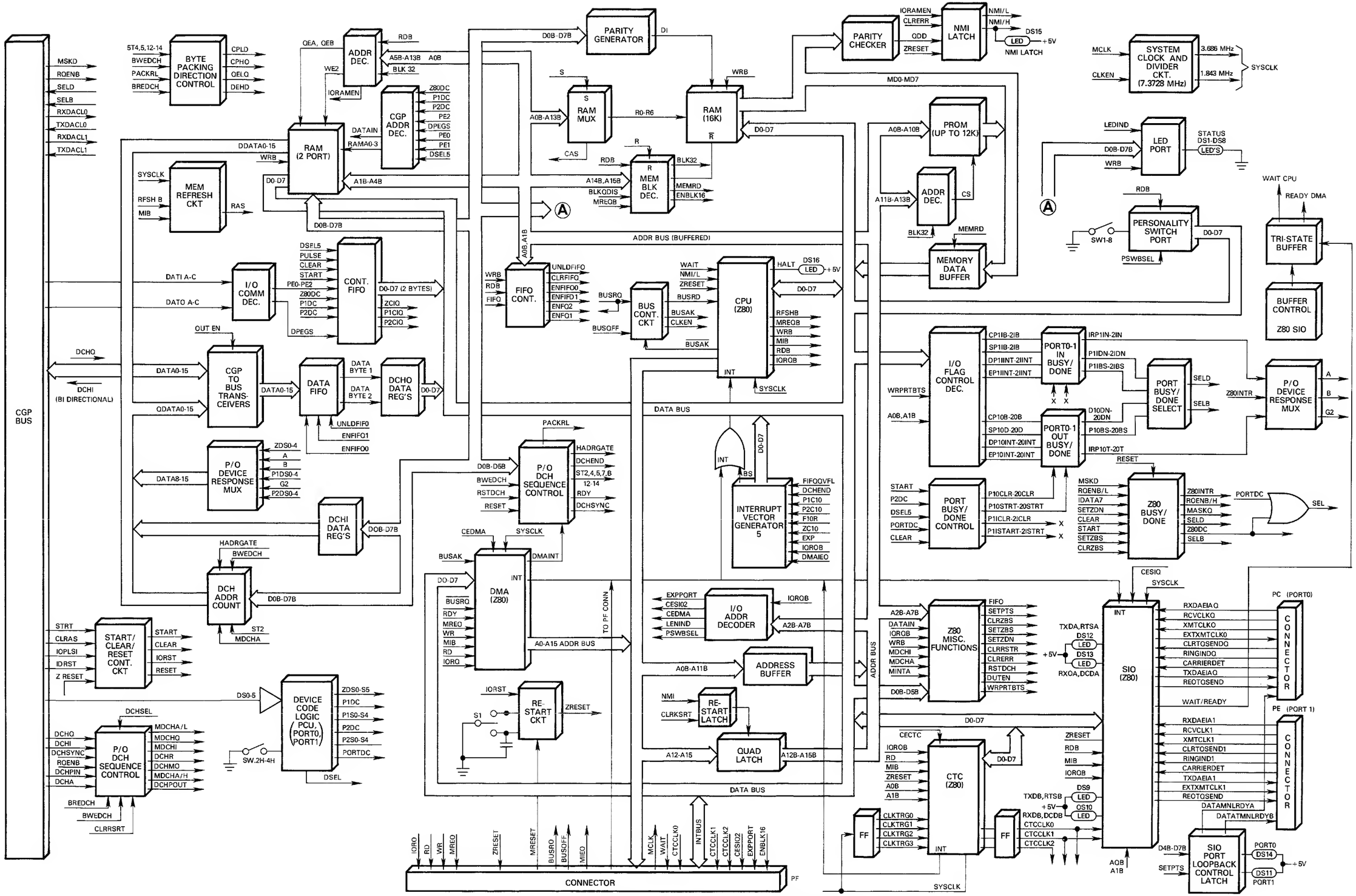


Programmable Communications Unit (PCU)

Logic Diagrams

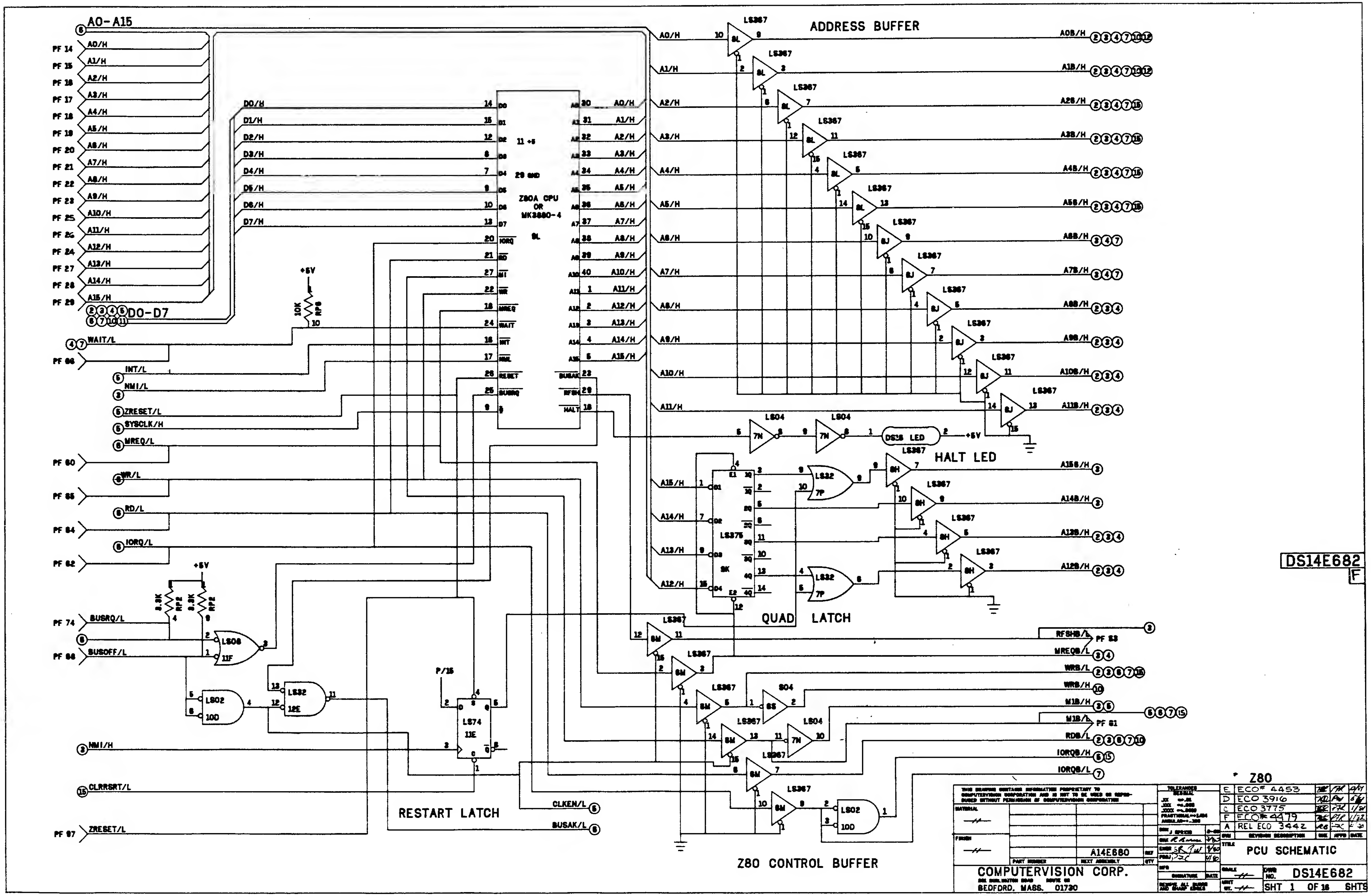
Order No. 001-00540-003

Table of Contents



Programmable Communications Unit Simplified Block Diagram

Programmable Communications Unit
(New)
DS14E682


A0-A15
D0-D7
Z80A CPU OR MK3880-4
ADDRESS BUFFER
HALT LED
DS18 LED
QUAD LATCH
RESTART LATCH
Z80 CONTROL BUFFER
WAIT/L
INT/L
NMI/L
ZRESET/L
SYSCLK/H
MREQ/L
WR/L
RD/L
IORQ/L
BUSRQ/L
BUSOFF/L
NMI/H
CLRRSRT/L
ZRESET/L
CLKEN/L
BUSAK/L
RFSHB/L
MREQB/L
WRB/L
WRB/H
M1B/H
M1B/L
RDB/L
IORQB/H
IORQB/L
DS14E682
F
Z80
E ECO# 4453
D ECO 3916
C ECO 3775
F ECO# 4479
A REL ECO 3442
A14E680
PCU SCHEMATIC
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
DS14E682
SHT 1 OF 16 SHTS

A1B-A4B
RAMA0-RAMA3
D0B-D7B
Z80 ODD ADR
Z80 EVEN ADR
WRB/L
P/10
+5V
2.2K R10
OE-A/L
LS10
CGP LATCH ENABLE
A9B/H
BLK32/L
A5B/H
A6B+A7B/H
A8B/H
A9B/H
A10B/H
A11B/H
A12B/H
A13B/H
LS27
LS04
LS32
LS10
ADR DECODER
RDB/L
IORAMEN/H
IORAMEN/L
TTL IORAMEN/L
PF 11
5K
5L
7K
7L
29706
D0-D7
ODATA0-ODATA15
DS14E682
F
P/1
P/2
P/3
P/4
P/5
P/6
P/7
P/8
P/9
P/10
P/11
P/12
P/13
P/14
P/15
P/16
P/17
TWO PORT RAM
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
SEE SHEET 1
PCU SCHEMATIC
DWG NO. DS14E682
SHT 2 OF 18 SHTS

WRB/L

A3B/H
A10B/H
A2B/H
A9B/H
A1B/H
A8B/H
A0B/H
A7B/H

LS257A 6F

RAM MUX
LOGIC 0=A
INPUTS

4116 5E
4116 5D
4116 5C
4116 6E
4116 6D

D0/H MD0/H
D1/H MD1/H
D2/H MD2/H
D3/H MD3/H
D4/H MD4/H

MD0/H
MD7/H
MD6/H
MD5/H
MD4/H
MD3/H
MD2/H
MD1/H

S280 8F

PARITY CHECKER
MD0-MD7

A6B/H
A13B/H
A4B/H
A11B/H
A5B/H
A12B/H
P/5

LS257A 7F

4116 9C
4116 7E
4116 7D
4116 7C

D5/H MD5/H
D6/H MD6/H
D7/H MD7/H

D0B/H
D1B/H
D2B/H
D3B/H
D4B/H
D5B/H
D6B/H
D7B/H

S280 8E

PARITY GENERATOR

RAM MUX

S32 8C
DELAY

D0-D7

RDB/L

LS139 8D

BLK0/L
BLK32/L
BLK16/L

MEMORY BLOCK
DECODER

A15B/H
A14B/H
P/1
P/3

LS08 9D
LS02 10D
LS10 11C

PF 58 BLK0015/L

IORAMEN/L

8.2K RB1
+5V

S32 8C

MEMRD/L
NMI/L
NMI/H

LS367 8G

LS74 8C

DS15 LED

NMI LATCH

+5V
RP2
PF56

ENBLK16/L PF 12

16K RAM
BLOCK 0

MREQB/L
SYSCLK/H
RFSHB/L
M1B/H

LS04 7N

LS74 9C
LS74 10C
LS74 10C

MEMORY
REFRESH

8.2K RB0
8.2 RP1

CLRERR/L
ZRESET/L

LS10 11C

LS132 12C

DS14E682
F

SEE SHEET 1

PCU SCHEMATIC

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

DWG NO. DS14E682

SHT 3 OF 16 SHTS

MD0-MD7

ZRESET/L
IORAMEN/H
MREQB/L
SYSCLK/H
LS27
LS74
LS74
74S8
WAIT/L
P/12

DATA BUFFER
LS367
MD0/H
MD1/H
MD2/H
MD3/H
MD4/H
MD5/H
MD6/H
MD7/H
D0/H
D1/H
D2/H
D3/H
D4/H
D5/H
D6/H
D7/H
MEMRD/L
10K RPS

A13B/H
A12B/H
A11B/H
BLK32/L
LS138
E PROM ADR DECODER
F/5

A0B/H
A1B/H
A2B/H
A3B/H
A4B/H
A5B/H
A6B/H
A7B/H
A8B/H
A9B/H
A10B/H
2516
9000-97FF
9800-9FFF
A000-A7FF
A800-AFFF
B000-B7FF
B800-BFFF
A0B-A10B

PF 30
PF 31
PF 32
PF 33
PF 36
PF 35
PF 37
PF 34
D0-D7

+5V

D08/H
D18/H
D28/H
D38/H
D58/H
D68/H
D78/H
D48/H
PF 38
PF 39
PF 40
PF 41
PF 43
PF 44
PF 45
PF 42
E PROMS

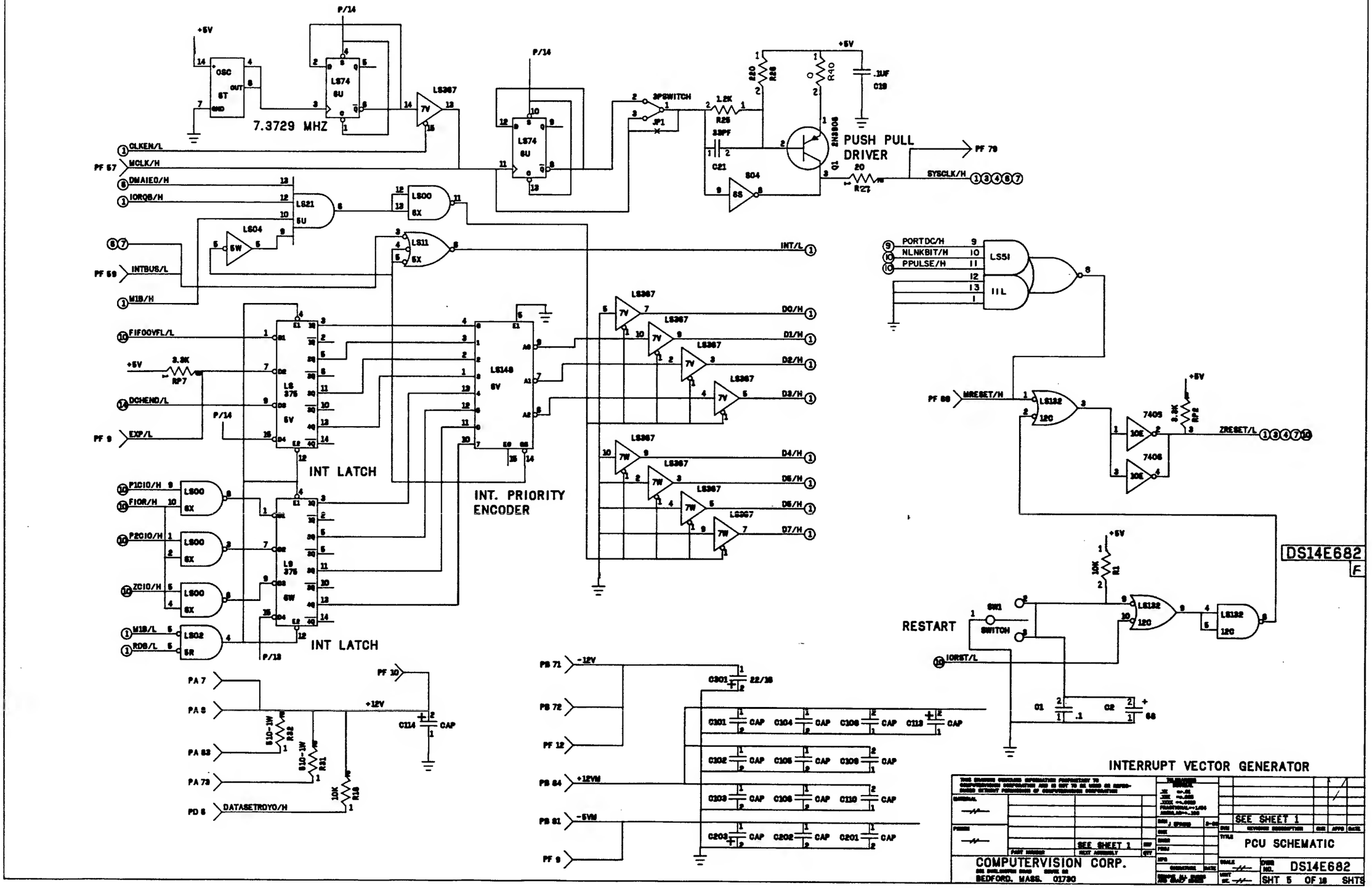
DS14E682
F

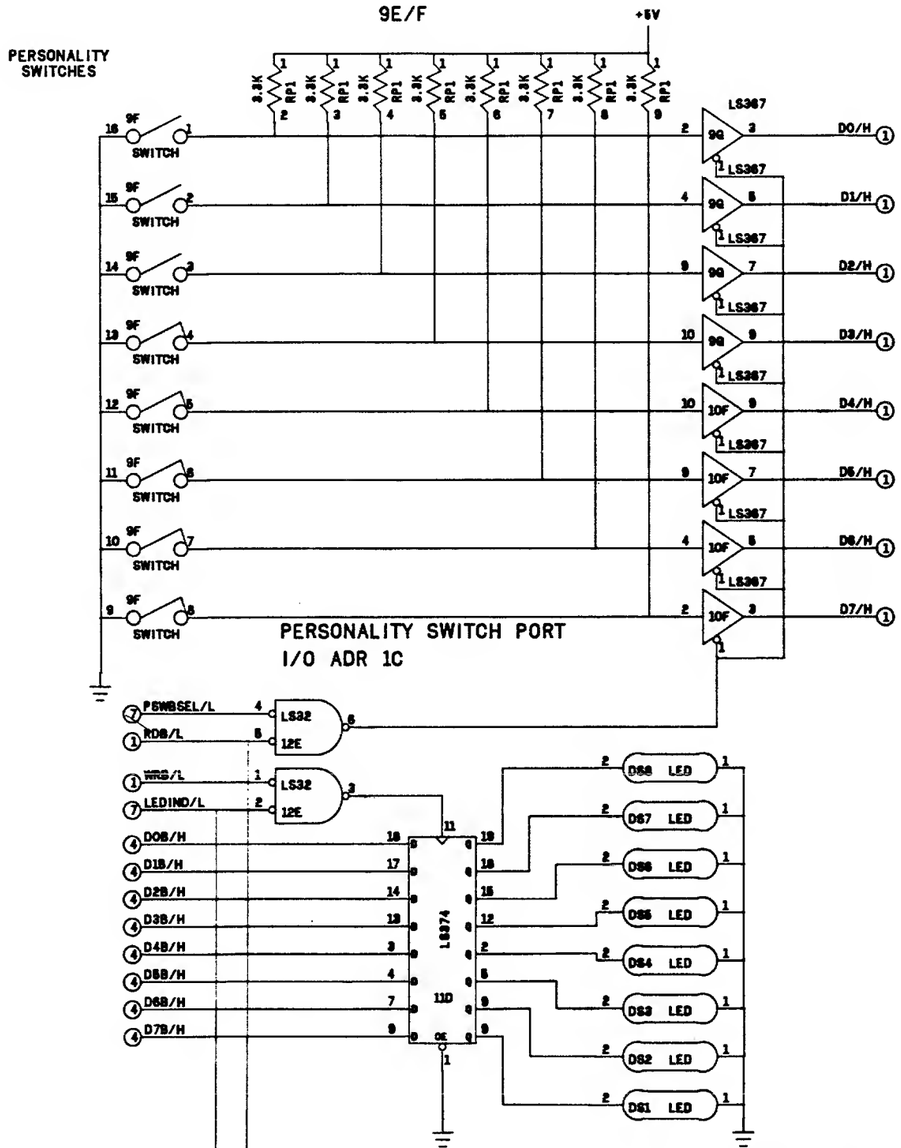
SEE SHEET 1

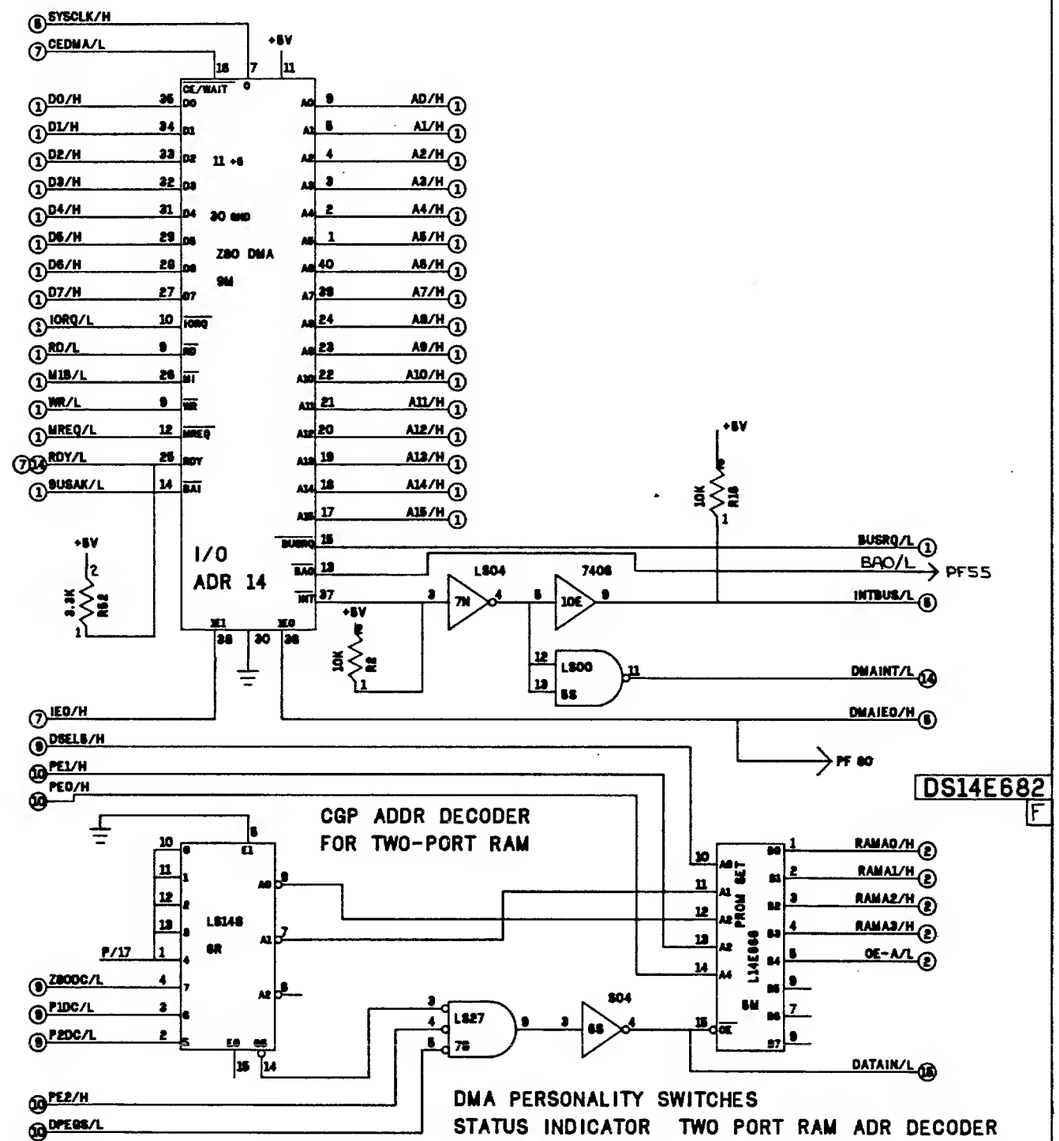
COMPUTERVISION CORP.
BEDFORD, MASS. 01730

PCU SCHEMATIC

DWG NO. DS14E682
SHT 4 OF 18 SHTS


7.3729 MHZ
PUSH PULL DRIVER
INT LATCH
INT. PRIORITY ENCODER
INT LATCH
RESTART
INTERRUPT VECTOR GENERATOR
DS14E682
F
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
PCU SCHEMATIC
SEE SHEET 1
SHT 5 OF 18 SHTS





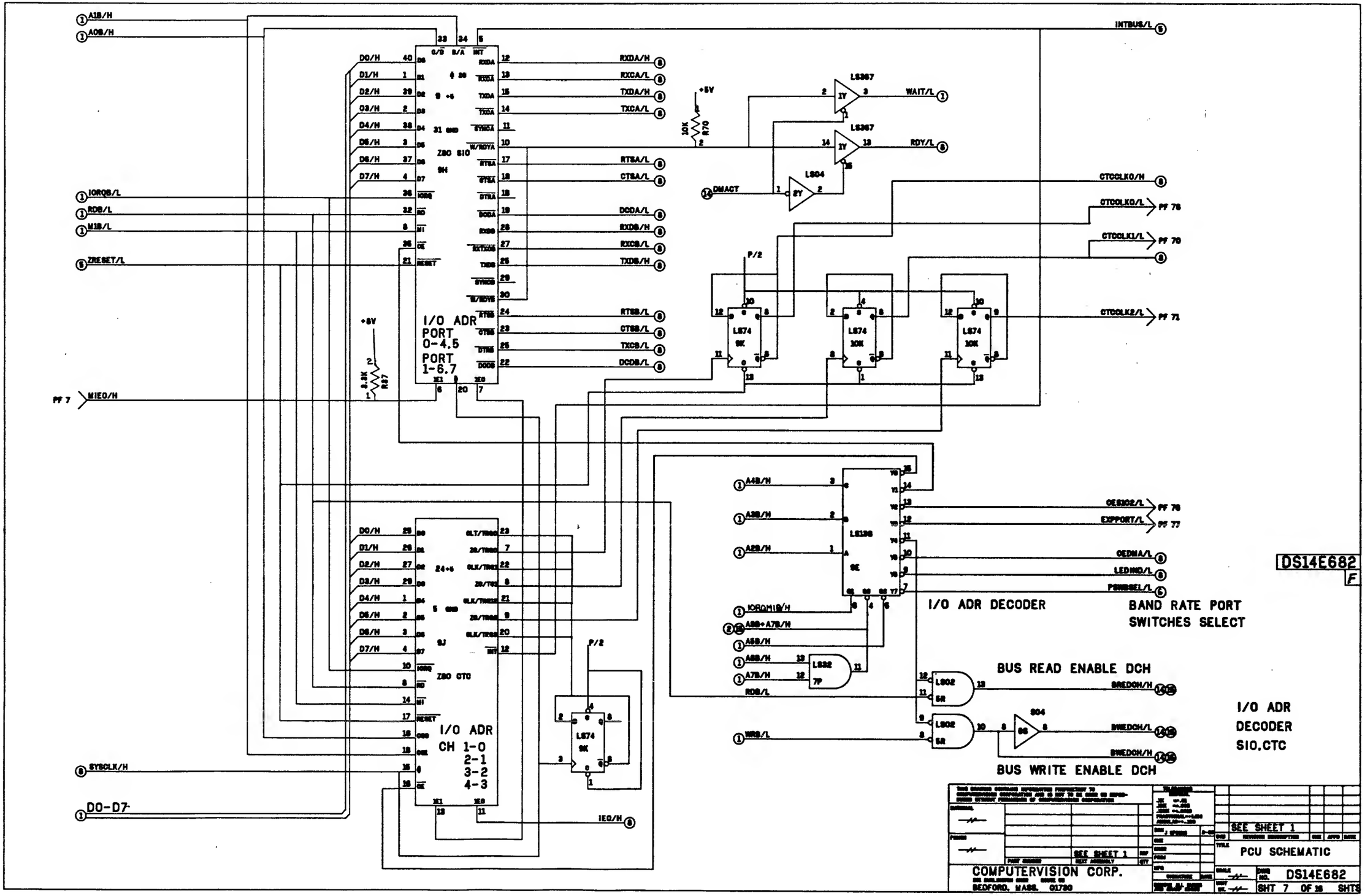
SEE SHEET 1

PCU SCHEMATIC

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

DWG NO. DS14E682

SHT 6 OF 18 SHTS


A1B/H
A0B/H
IORQB/L
RDB/L
M1B/L
ZRESET/L
PF 7
MIEO/H
SYSCLK/H
D0-D7
IEO/H
INTBUS/L
D0/H
D1/H
D2/H
D3/H
D4/H
D5/H
D6/H
D7/H
Z80 SIO
9H
I/O ADR
PORT
0-4.5
PORT
1-6.7
RXDA/H
RXCA/L
TXDA/H
TXCA/L
RTSA/L
CTSA/L
DCDA/L
RXDB/H
RXCB/L
TXDB/H
RTSB/L
CTSB/L
TXCB/L
DCDB/L
+5V
10K
R70
LS367
WAIT/L
RDY/L
LS04
DMACT
CTCCLKO/H
CTCCLKO/L
PF 78
CTCCLKI/L
PF 79
CTCCLK2/L
PF 71
P/2
LS74
9K
10K
8.2K
R87
Z80 CTC
9J
I/O ADR
CH 1-0
2-1
3-2
4-3
A4B/H
A3B/H
A2B/H
IORQM1B/H
A8B+A7B/H
A5B/H
A6B/H
A7B/H
RDB/L
WRB/L
LS138
9K
LS32
7P
OESIO2/L
EXPPORT/L
PF 76
PF 77
GEDMA/L
LEDMD/L
PSWBSEL/L
I/O ADR DECODER
BAND RATE PORT
SWITCHES SELECT
BUS READ ENABLE DCH
LS02
BREDOH/H
BREDOH/L
LS04
I/O ADR
DECODER
SIO,CTC
BUS WRITE ENABLE DCH
DS14E682
F
SEE SHEET 1
PCU SCHEMATIC
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
DS14E682
SHT 7 OF 18 SHTS

RXDA.DCDA

TXDA.RTSA

S10 PORT 1
LOOPBACK MUX

RXDB.DCDB

TXDB.RTSB
SIO PORT 1

SIO COMMUNICATIONS INTERFACE

SIO PORT
LOOPBACK
CONTROL LATCH
I/O ADR 20

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

PCU SCHEMATIC

DS14E682

SHT 8 OF 16 SHTS

DEVICE SELECT PCU

DEVICE SELECT PORT 1

CLOSE TO DISABLE PORT 0

CLOSE TO DISABLE PORT 1

DEVICE CODE LOGIC Z80 BUSY/DONE

DS14E682

F

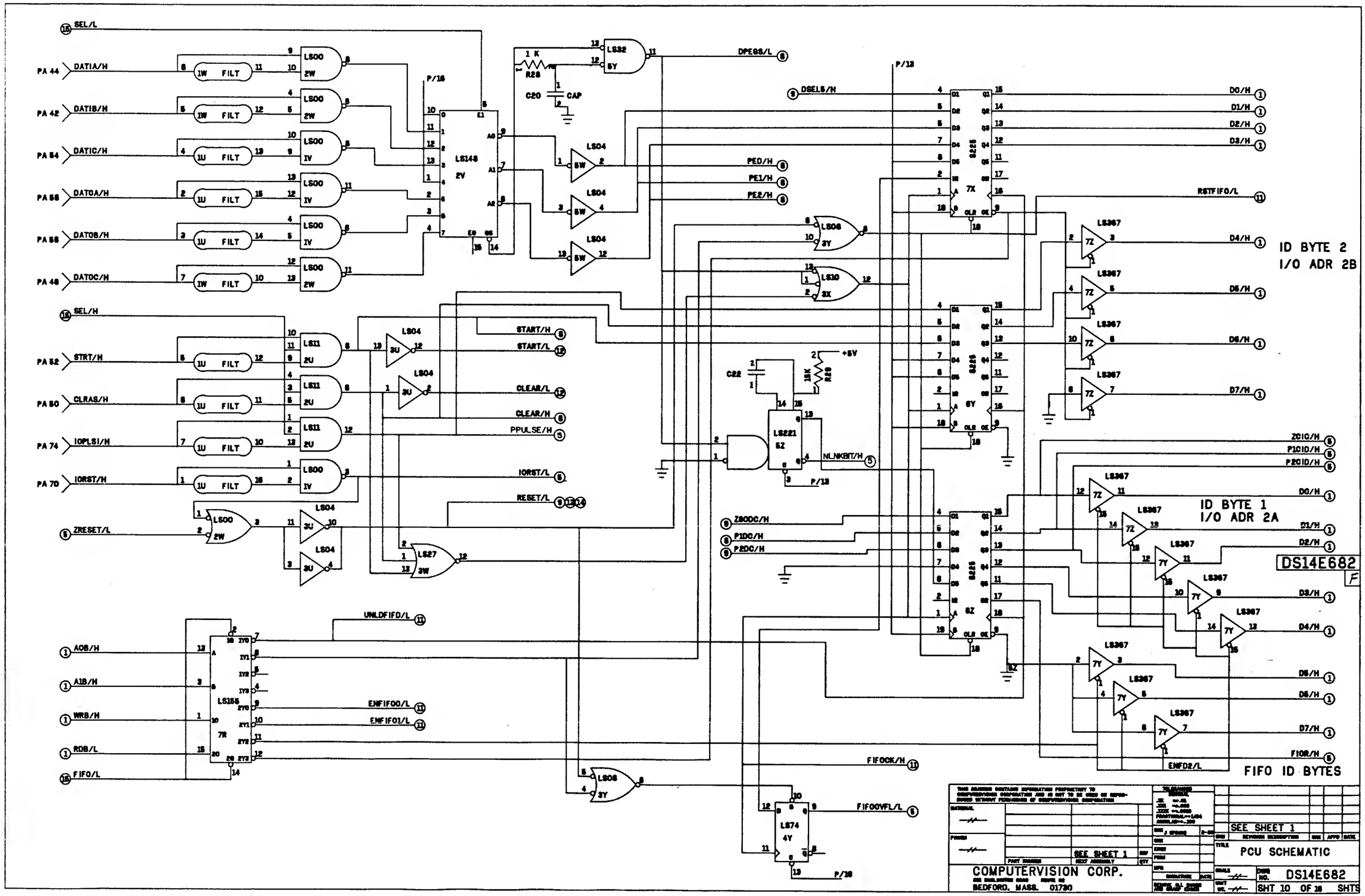
SEE SHEET 1

PCU SCHEMATIC

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

DWG NO. DS14E682

SHT 9 OF 16 SHTS


SEL/L
PA 44
DATIA/H
PA 42
DATIB/H
PA 54
DATIC/H
PA 56
DATOA/H
PA 58
DATOB/H
PA 48
DATOC/H
FILT
LS00
LS148
P/16
1 K
R28
C20
CAP
LS32
DPEOS/L
DSELS/H
PED/H
PE1/H
PE2/H
LS04
LS08
LS10
P/13
8223
7X
8Y
8Z
LS367
RSTFIFO/L
D0/H
D1/H
D2/H
D3/H
D4/H
D5/H
D6/H
D7/H
ID BYTE 2
I/O ADR 2B
SEL/H
PA 52
STRT/H
PA 50
CLRAS/H
PA 74
IOPLSI/H
PA 70
IORST/H
ZRESET/L
LS11
LS27
START/H
START/L
CLEAR/L
CLEAR/H
PPULSE/H
IORST/L
RESET/L
C22
15K
R29
+5V
LS221
NLNKBIT/H
Z80DC/H
P1DC/H
P2DC/H
ZCIC/H
P1CID/H
P2CID/H
ID BYTE 1
I/O ADR 2A
DS14E682
F
AOB/H
A1B/H
WRB/H
RDB/H
FIFO/L
LS155
7R
UNLDFIFO/L
ENFIFO0/L
ENFIFO1/L
LS08
FIFOCK/H
LS74
4Y
FIFOOVFL/L
ENFD2/L
FIFO ID BYTES
SEE SHEET 1
PCU SCHEMATIC
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
DWG NO. DS14E682
SHT 10 OF 18 SHTS

FIFO BYTE 1
I/O ADR 28
(LOW ORDER)

FIFO
BYTE 2
I/O ADR 29
(HIGH ORDER)

CGP TO BUS
TRANSCEIVERS

DCHI DATA REGISTERS

DATA FIFO DCH REGISTERS

DS14E682
F

SEE SHEET 1

PCU SCHEMATIC

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

DS14E682

SHT 11 OF 16 SHTS

DEVICE RESPONSE MUX

P1DS0/H
ZDS0/H
P2DS0/H
P/S
ZDS1/H
P1DS1/H
P2DS1/H
LS253 4D
LS367 7M
ODATA8/H
ODATA9/H
ODATA10/H
ODATA11/H

P1DS2/H
ZDS2/H
P2DS2/H
ZDS3/H
P1DS3/H
P2DS3/H
LS253 3D
ODATA12/H
ODATA13/H

P1DS4/H
ZDS4/H
P2DS4/H
LS253 2D
ODATA14/H
ODATA15/H

PCUMSK/H
P/S
IRP2OT/L
IRP1OT/L
IRP2IN/L
IRP1IN/L
Z80INTR/L
LS148 1J
LS04 6Y
7406 6T
INTR/L
PB 29

D0B/H
A0B/H
A1B/H
WRPRTBTS/H
WRPRTBTS/L
D1B/H
D2B/H
D3B/H
D4B/H
D5B/H
D6B/H
D7B/H
LS04 4S 4R
LS155 2S 2T 1R
CP11B/L
CP21B/L
SP11D/L
SP21D/L
DP11INT/L
DP21INT/L
EP11INT/L
EP21INT/L
CP10B/L
CP20B/L
SP10D/L
SP20D/L
DP10INT/L
DP20INT/L
EP10INT/L
EP20INT/L

I/O FLAG CONTROL DECODER

P20DN/H
P10DN/H
P11DN/H
P21DN/H
P10BS/H
P20BS/H
P11BS/H
P21BS/H
DSELB/L
P1DC/L
LS253 2R
7438 4T
SELD/L
SELB/L

PORT BUSY / DONE SELECT

PA 96 INTPIN/L
PA 40 INTA/H
LS04 2Y
1W FILT
LS08 3Y
LS11 3X
MINTA/L
MINTA/H

INT PRIORITY

+5V
330 R24
7438 4T
INTPOUT/L
PA 96
390 R28

START/L
P2DC/H
DSELB/H
PORTDC/H
PORTDC/L
CLEAR/L
LS258 2P
P1ISTRT/L
P2ISTRT/L
P1OSTRT/L
P2OSTRT/L
P1CLR/L
P2CLR/L
P1OCLR/L
P2OCLR/L

PORT BUSY/ DONE CONTROL

PORT 0,1-CGP INTERFACE

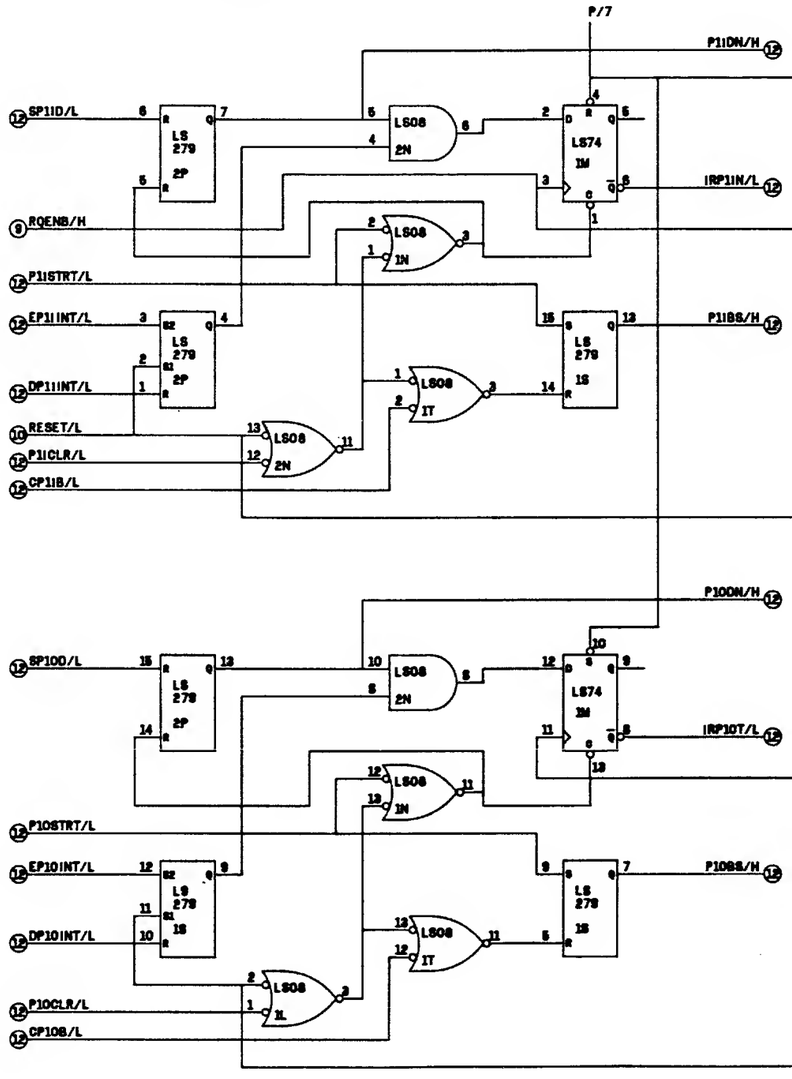
DS14E682
F

SEE SHEET 1
SEE SHEET 1

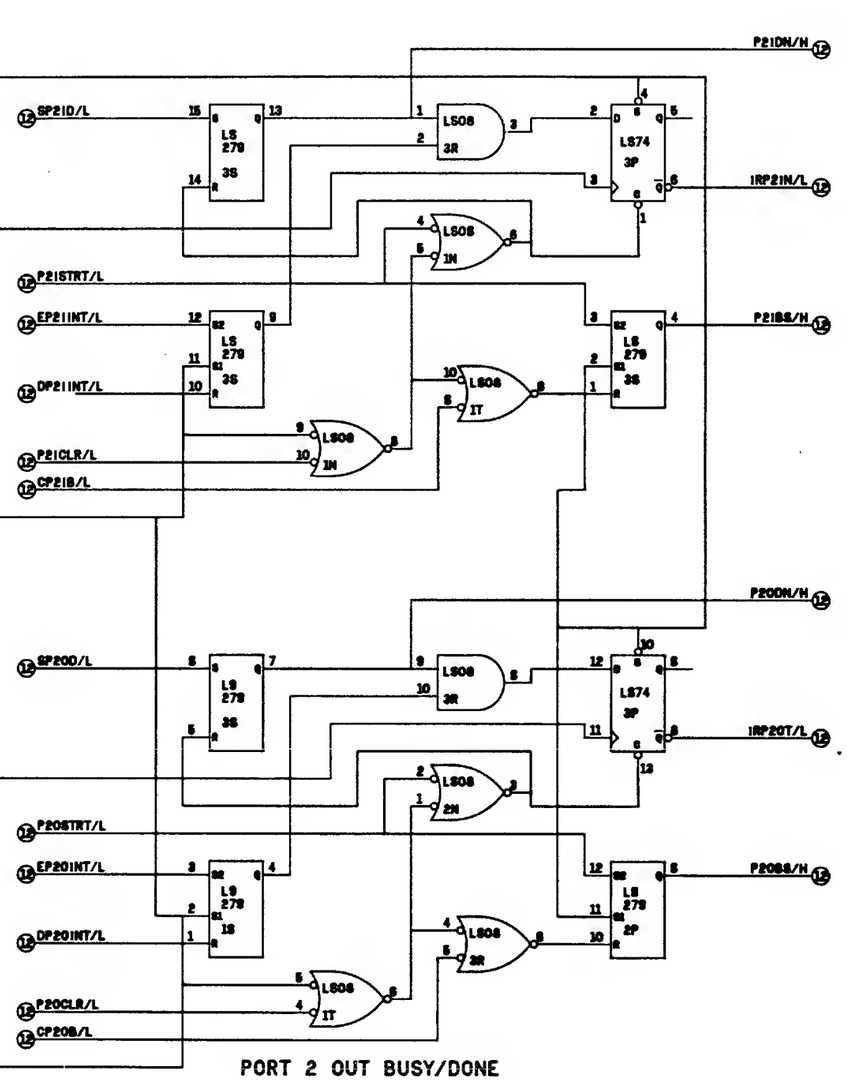
COMPUTERVISION CORP.
BEDFORD, MASS. 01730

TITLE PCU SCHEMATIC
DWG NO. DS14E682
SHT 12 OF 16 SHTS

PORT 0 IN BUSY/DONE



PORT 1 IN BUSY/DONE



PORT 2 OUT BUSY/DONE

PORT 0 OUT BUSY/DONE

PORT 0-1 BUSY/DONE

DS14E682
F

SEE SHEET 1

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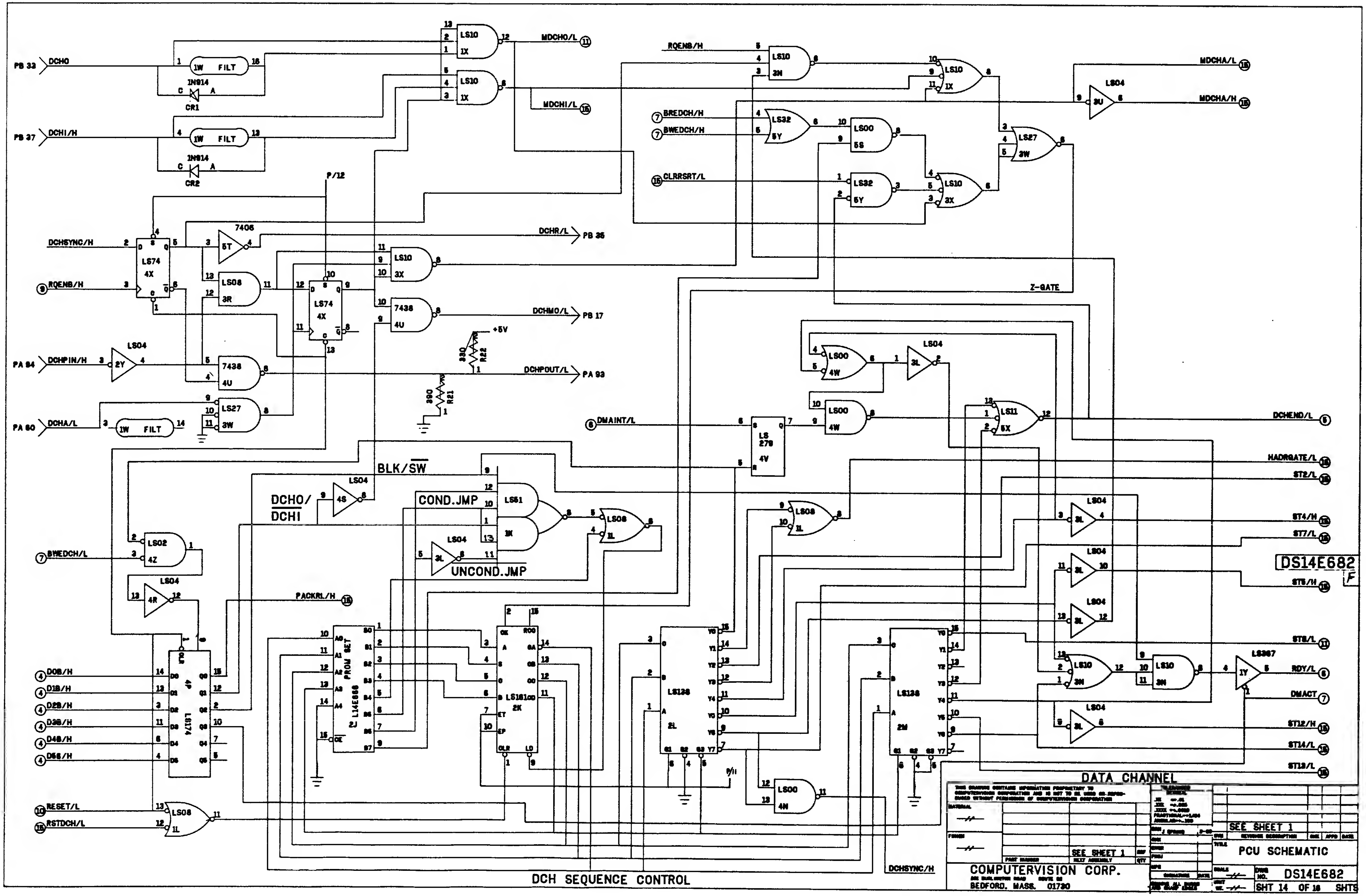
BEDFORD, MASS. 01730

TITLE: PCU SCHEMATIC

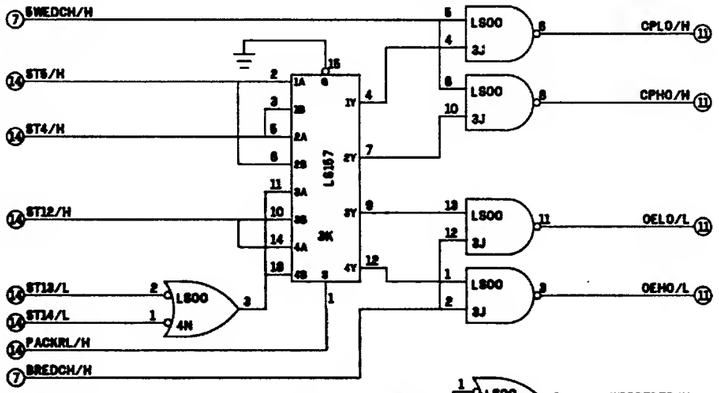
DWG NO. DS14E682

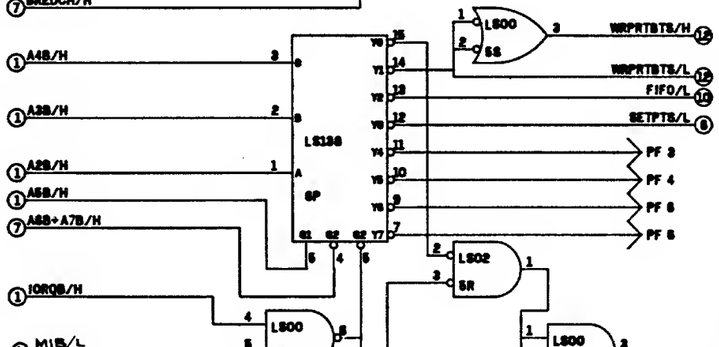
SHT 13 OF 18 SHTS

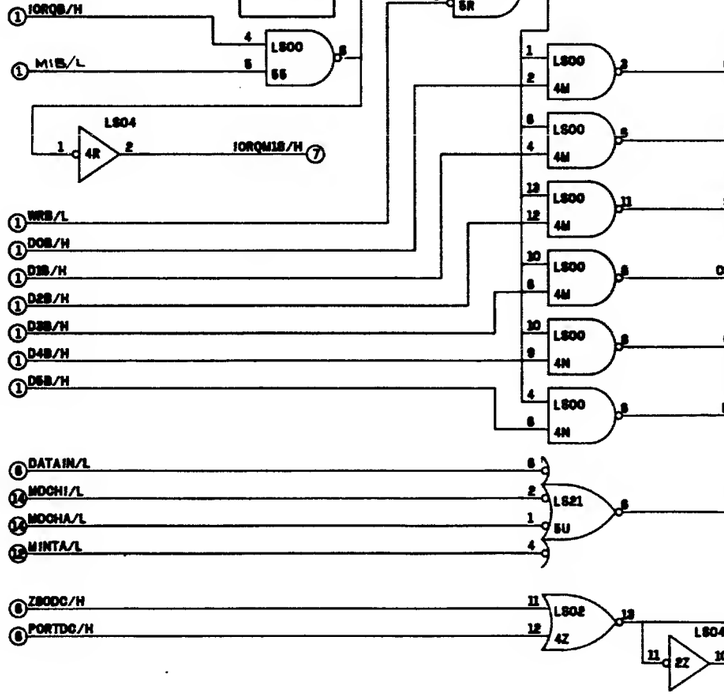


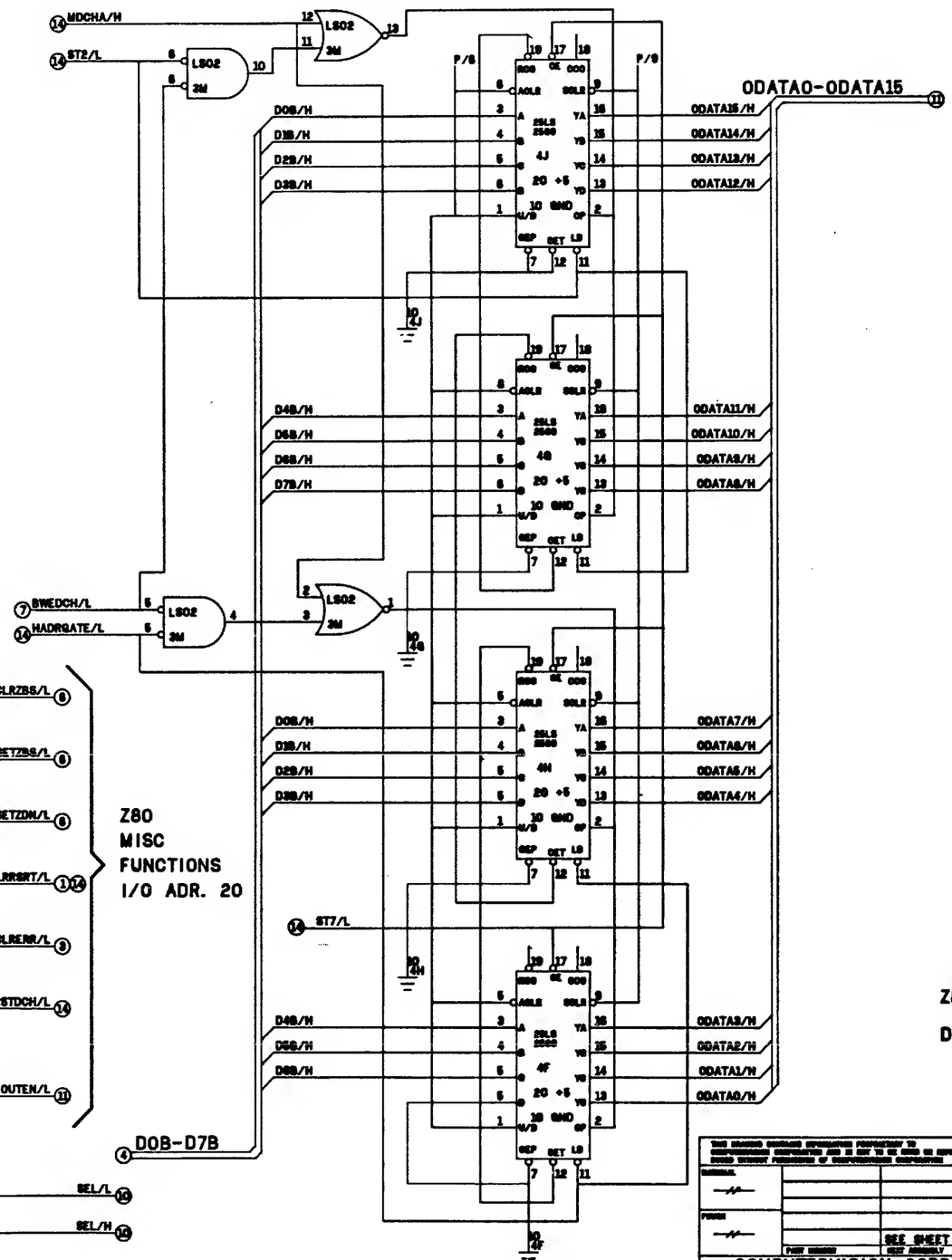
MDCHO/L
MDCHI/L
MDCHA/L
MDCHA/H
RQENB/H
BREDCH/H
BWEDCH/H
CLRRSRT/L
DCHO
DCHI/H
FILT
1N914
CR1
CR2
P/12
DCHSYNC/H
RQENB/H
DCHR/L
DCHMO/L
DCHPIN/H
DCHPOUT/L
DCHA/L
+5V
Z-GATE
DMAINT/L
DCHEND/L
HADRGATE/L
ST2/L
ST4/H
ST7/L
ST5/H
ST8/L
RDY/L
DMACT
ST12/H
ST14/L
ST13/L
BLK/SW
COND.JMP
UNCOND.JMP
DCHO/
DCHI
PACKRL/H
BWEDCH/L
PROM SET
D0B/H
D1B/H
D2B/H
D3B/H
D4B/H
D5B/H
RESET/L
RSTDCH/L
DCHSYNC/H
DCH SEQUENCE CONTROL
DS14E682
DATA CHANNEL
SEE SHEET 1
PCU SCHEMATIC
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
DS14E682
SHT 14 OF 18 SHTS

BYTE PACKING DIRECTION CONTROL









DS14E682
E

Z80 MISC FUNCTIONS
DCH ADDER COUNTER

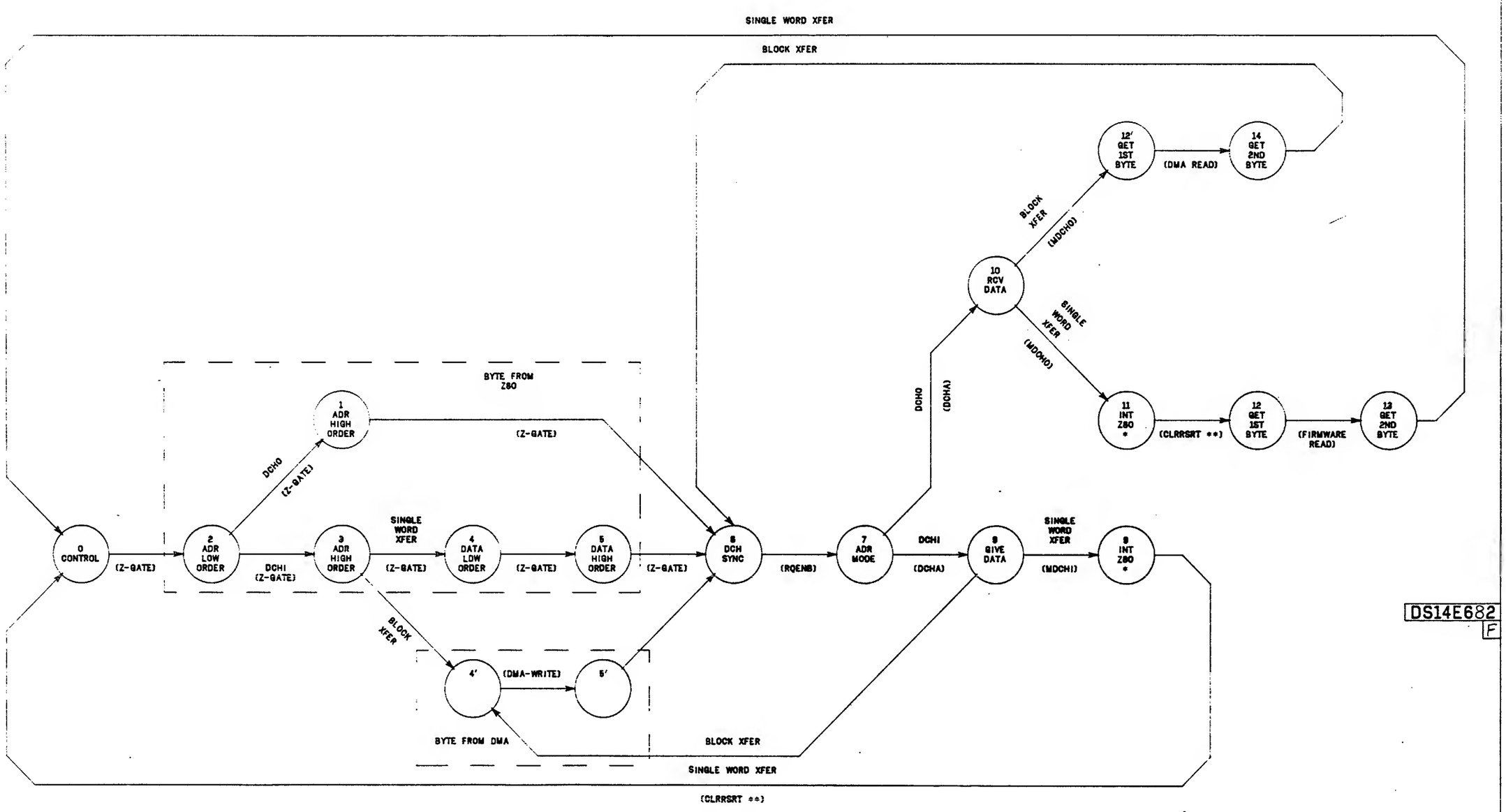
SEE SHEET 1

PCU SCHEMATIC

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

DS14E682

SHT 15 OF 19 SHTS



DS14E682
F

* DCHEND INT

** CLEARS DCH INT

SIGNALS IN PARENTHESES CAUSE THE STATES TO ADVANCE.

DATA CHANNEL CONTROLLER STATE DIAGRAM

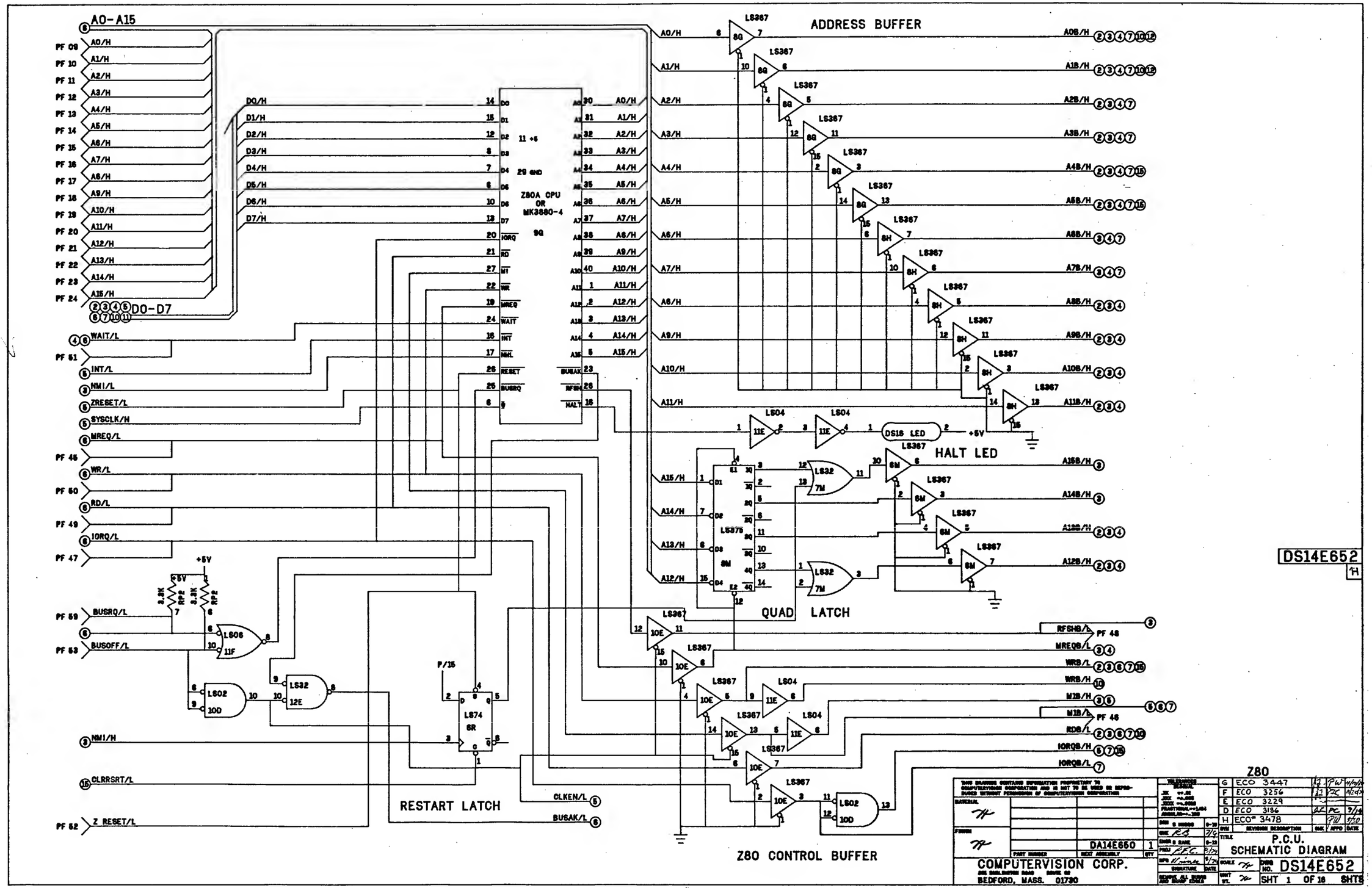
COMPUTERVISION CORP.
BEDFORD, MASS. 01730

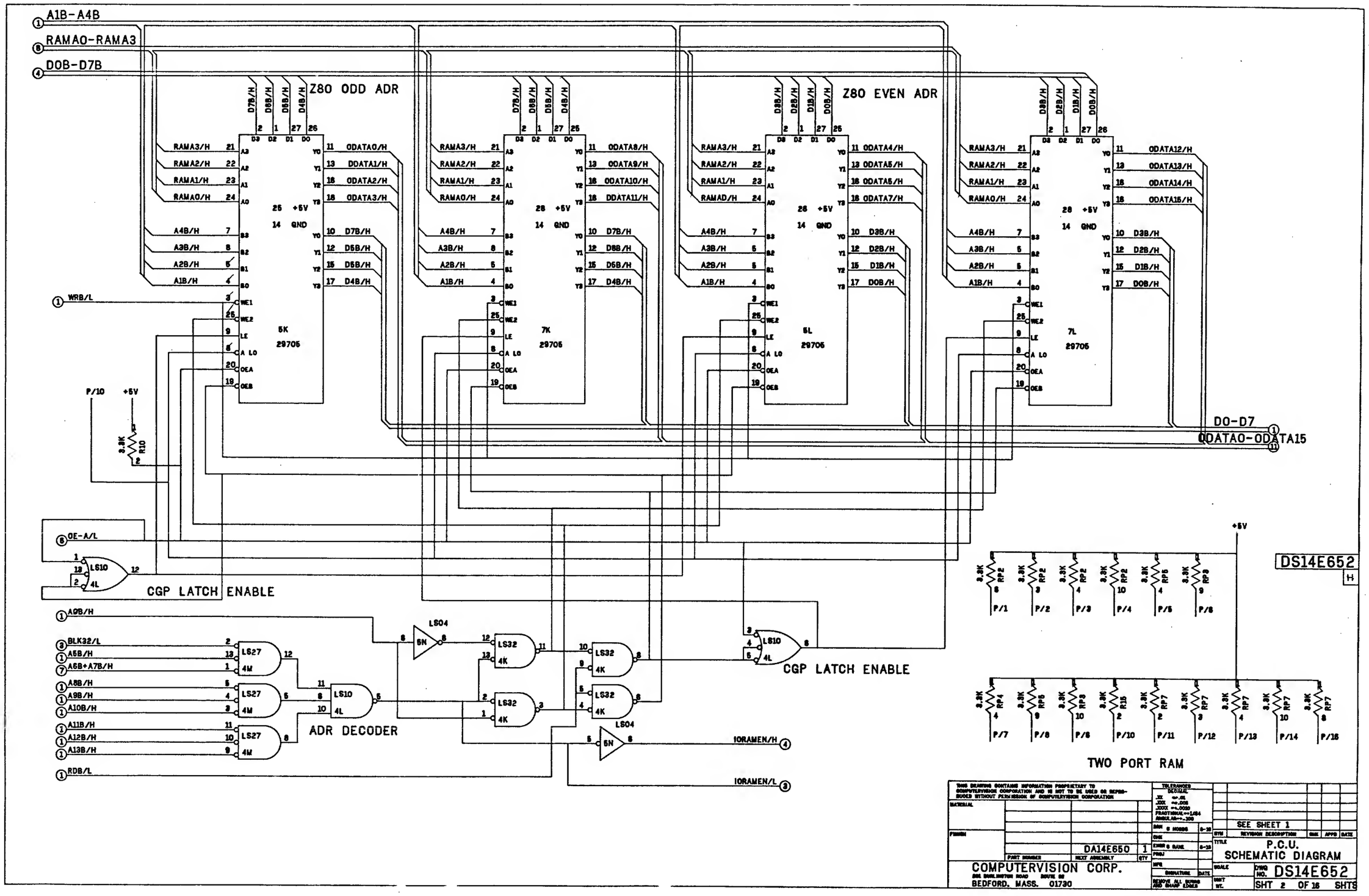
P.C.U.
SCHEMATIC DIAGRAM

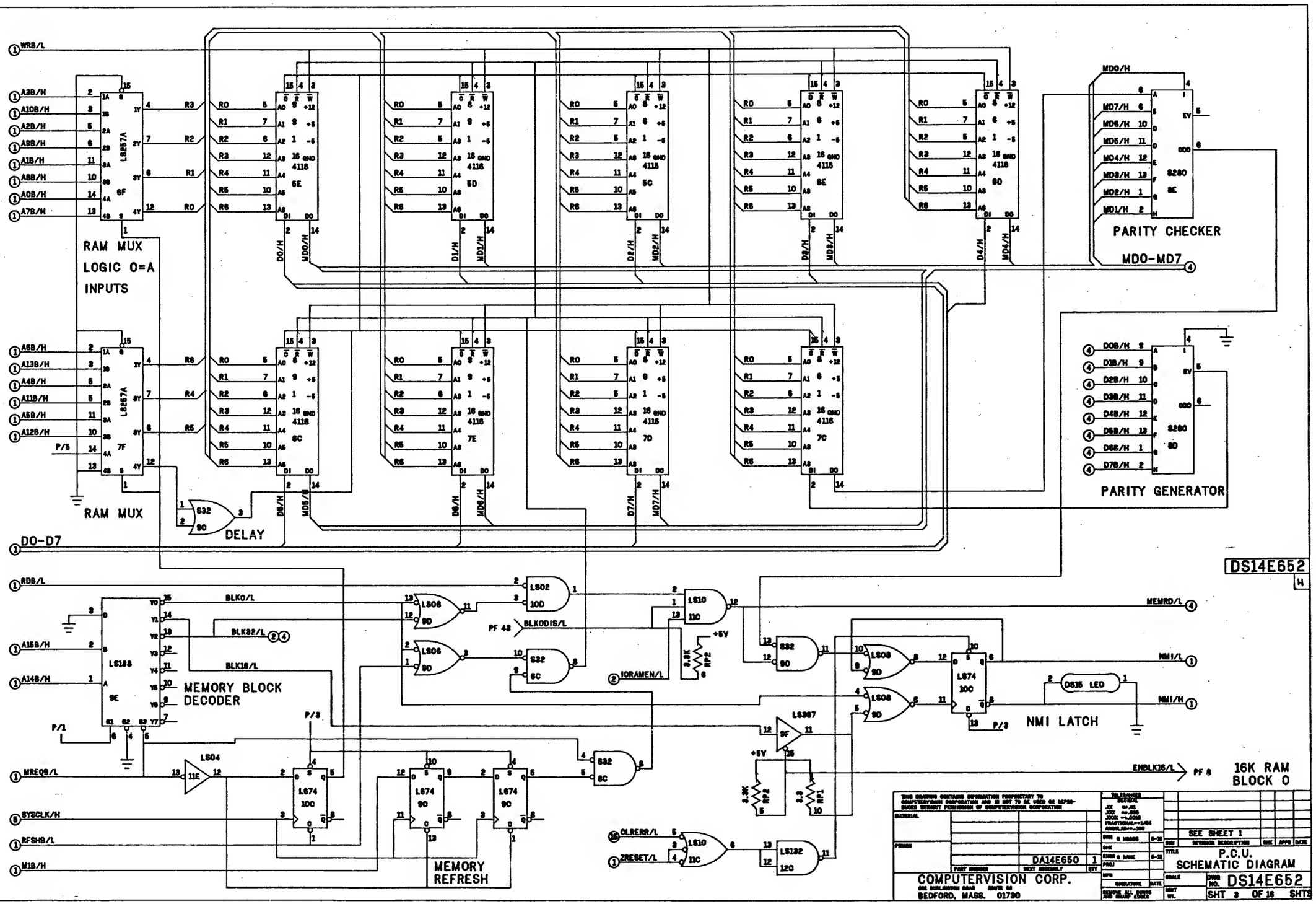
DWG NO. DS14E682

SHT 16 OF 16 SHTS

Programmable Communications Unit
(Obsolete)
DS14E652


A0-A15
D0-D7
WAIT/L
INT/L
NMI/L
ZRESET/L
SYSCLK/H
MREQ/L
WR/L
RD/L
IORQ/L
+5V
BUSRQ/L
BUSOFF/L
NMI/H
CLRRSRT/L
Z RESET/L
Z80A CPU OR MK3880-4
9Q
RESTART LATCH
CLKEN/L
BUSAK/L
Z80 CONTROL BUFFER
ADDRESS BUFFER
LS367
HALT LED
DS18 LED
QUAD LATCH
LS375
RFSHB/L
MREQB/L
WRB/L
WRB/H
M1B/H
M1B/L
RDB/L
IORQB/H
IORQB/L
DS14E652
Z80
P.C.U.
SCHEMATIC DIAGRAM
DA14E650
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
SHT 1 OF 16 SHTS


A1B-A4B
RAMA0-RAMA3
D0B-D7B
Z80 ODD ADR
Z80 EVEN ADR
D7B/H
D6B/H
D5B/H
D4B/H
D3B/H
D2B/H
D1B/H
D0B/H
RAMA3/H
RAMA2/H
RAMA1/H
RAMA0/H
RAMAD/H
A4B/H
A3B/H
A2B/H
A1B/H
ODATA0/H
ODATA1/H
ODATA2/H
ODATA3/H
ODATA4/H
ODATA5/H
ODATA6/H
ODATA7/H
ODATA8/H
ODATA9/H
ODATA10/H
DDATA11/H
ODATA12/H
ODATA13/H
ODATA14/H
ODATA15/H
D7B/H
D5B/H
D4B/H
D3B/H
D2B/H
D1B/H
D0B/H
26 +5V
14 GND
5K
29705
7K
29705
5L
29705
7L
29705
WRB/L
WE1
WE2
LE
A LO
OEA
OEB
P/10
+5V
3.3K
R10
D0-D7
ODATA0-ODATA15
OE-A/L
LS10
4L
CGP LATCH ENABLE
AGB/H
BLK32/L
A5B/H
A6B+A7B/H
A8B/H
A9B/H
A10B/H
A11B/H
A12B/H
A13B/H
RDB/L
LS27
4M
LS10
4L
ADR DECODER
LS04
6N
LS32
4K
IORAMEN/H
IORAMEN/L
CGP LATCH ENABLE
+5V
3.3K
RP2
RP5
RP8
RP4
R35
RP7
P/1
P/2
P/3
P/4
P/5
P/6
P/7
P/8
P/9
P/10
P/11
P/12
P/13
P/14
P/15
TWO PORT RAM
DS14E652
H
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION
TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL
.XX +-.01
.XXX +-.005
.XXXX +-.0050
FRACTIONAL +-1/64
ANGULAR +-.30
MATERIAL
FINISH
PART NUMBER
DA14E650
NEXT ASSEMBLY
1
QTY
SEE SHEET 1
REVISION DESCRIPTION
TITLE
P.C.U.
SCHEMATIC DIAGRAM
COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730
DWG NO. DS14E652
SHT 2 OF 16 SHTS


WR8/L
A2B/H
A10B/H
A2B/H
A9B/H
A1B/H
A8B/H
A0B/H
A7B/H
L8257A
6F
R3
R2
R1
R0
RAM MUX
LOGIC 0=A
INPUTS
A6B/H
A13B/H
A4B/H
A11B/H
A5B/H
A12B/H
P/5
7F
R6
R4
R5
RAM MUX
S32
9D
DELAY
D0-D7
RD8/L
A15B/H
A14B/H
LS138
9E
BLK0/L
BLK32/L
BLK16/L
MEMORY BLOCK
DECODER
P/1
P/3
MREQ8/L
LS04
11E
L674
10C
SYSCLK/H
RFSHB/L
M1B/H
MEMORY
REFRESH
5E
5D
5C
8E
8D
7E
7D
7C
8C
4116
D0/H
D1/H
D2/H
D3/H
D4/H
D5/H
D6/H
D7/H
MD0/H
MD1/H
MD2/H
MD3/H
MD4/H
MD5/H
MD6/H
MD7/H
PARITY CHECKER
MD0-MD7
S280
8E
PARITY GENERATOR
D0B/H
D1B/H
D2B/H
D3B/H
D4B/H
D5B/H
D6B/H
D7B/H
8D
LS02
10D
LS08
9D
LS10
11C
PF 43
BLKODIS/L
IORAMEN/L
+5V
8.2K
RP2
MEMRD/L
NMI1/L
NMI1/H
LS74
10C
DS15 LED
NMI LATCH
LS367
9F
ENBLK16/L
PF 8
16K RAM
BLOCK 0
CLRERR/L
ZRESET/L
LS132
12C
DS14E652
H
SEE SHEET 1
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
DA14E650
P.C.U.
SCHEMATIC DIAGRAM
DS14E652
SHT 3 OF 16 SHTS

MD0-MD7

ZRESET/L
IORAMEN/H
MREQB/L
SYSCLK/H
LS27 5T
LS74 3S
P/12
7438 3R
WAIT/L

DATA BUFFER
LS367 8J
MD0/H D0/H
MD1/H D1/H
MD2/H D2/H
MD3/H D3/H
MD4/H D4/H
MD5/H D5/H
MD6/H D6/H
MD7/H D7/H
MEMRD/L
+5V
10K RPS
LS367 8L
D0/H D1/H D2/H D3/H D4/H D5/H D6/H D7/H
D0B/H D1B/H D2B/H D3B/H D4B/H D5B/H D6B/H D7B/H
PF 33 PF 34 PF 35 PF 36 PF 39 PF 40 PF 37

E PROMS
LS367 8K
PF 25 D0/H
PF 26 D1/H
PF 27 D2/H
PF 28 D3/H
PF 30 D5/H
PF 31 D6/H
PF 32 D7/H
PF 29 D4/H
D0-D7

A0B/H A1B/H A2B/H A3B/H A4B/H A5B/H A6B/H A7B/H A8B/H A9B/H A10B/H
A0 A1 A8 A8 A4 A5 A6 A7 A8 A9 A30
CS
19+12 24+5 21-5 12 GND
DO0 DO1 DO2 DO3 DO4 DO5 DO6 DO7
2716

9000-97FF 5J
9800-9FFF 7J
A000-A7FF 5H
A800-AFFF 7H
B000-B7FF 5G
B800-BFFF 7G

9M00/H 10 M01/H 11M02/H 13M03/H 14M04/H 15M05/H 16M06/H 17M07/H
9MD0/H 10 M01/H 11M02/H 13M03/H 14M04/H 15M05/H 16MD6/H 17M07/H
5M00/H 10 M01/H 11M02/H 13M03/H 14M04/H 15M05/H 16MD6/H 17M07/H
8MD0/H 10 M01/H 11M02/H 13M03/H 14M04/H 15M05/H 16MD6/H 17M07/H

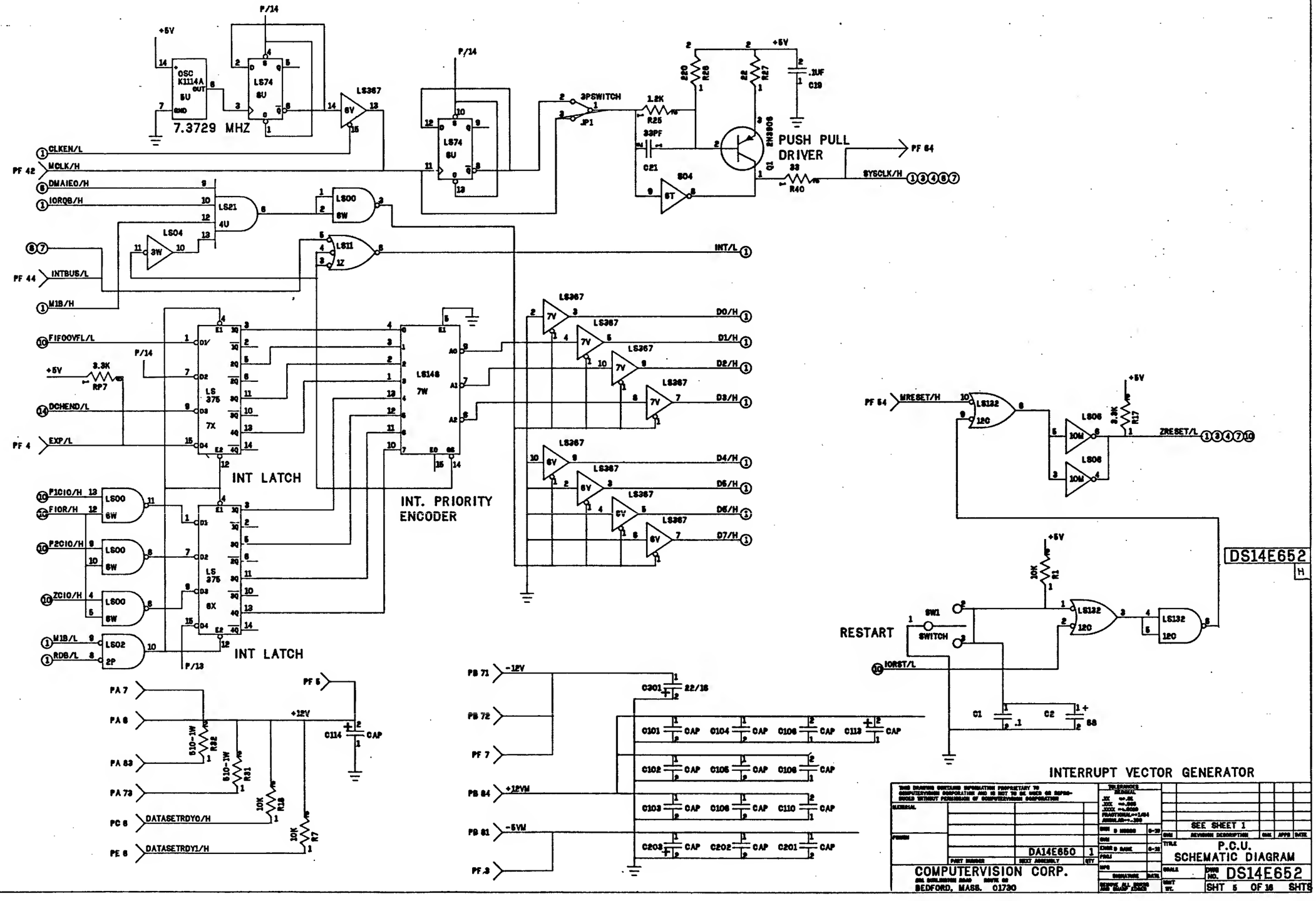
A0B-A10B
A11B/H A12B/H A13B/H BLK32/L
LS138 8F
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
E PROM ADR DECODER
P/5

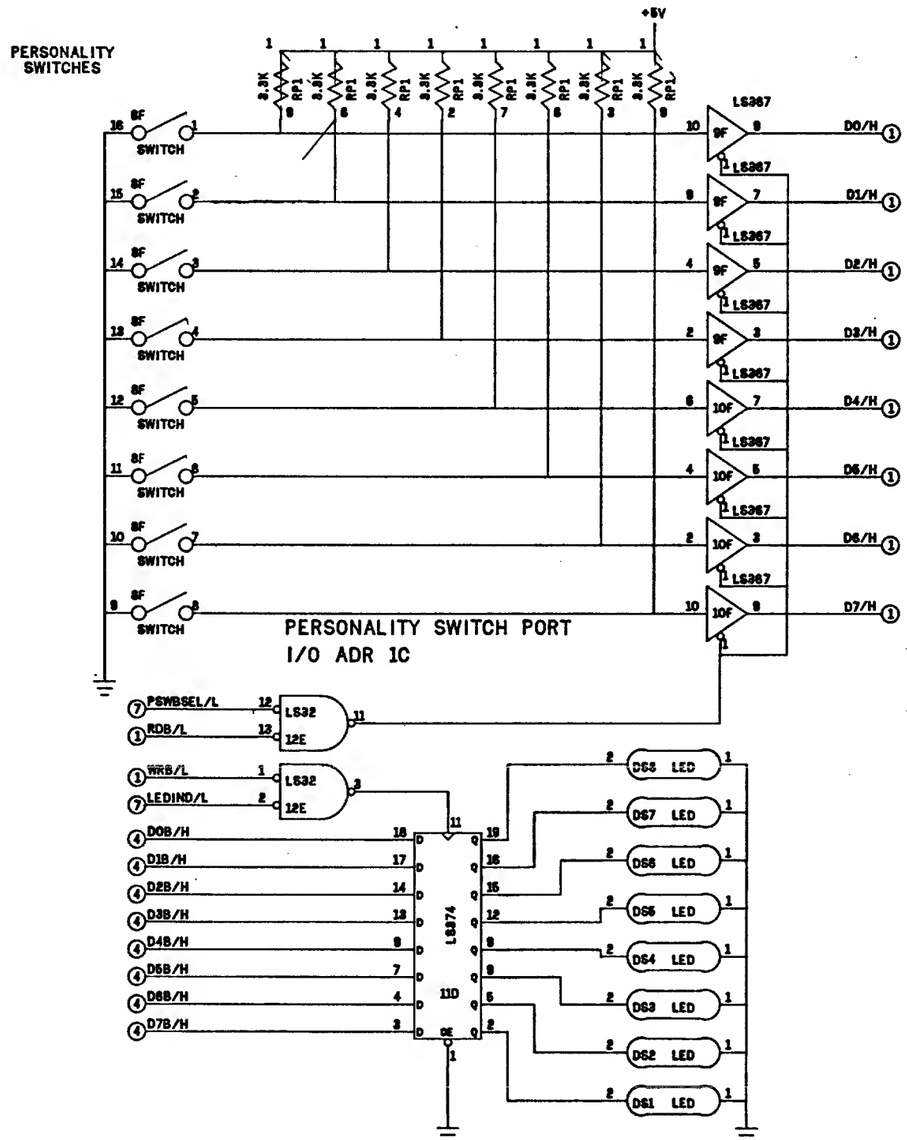
DS14E652 H

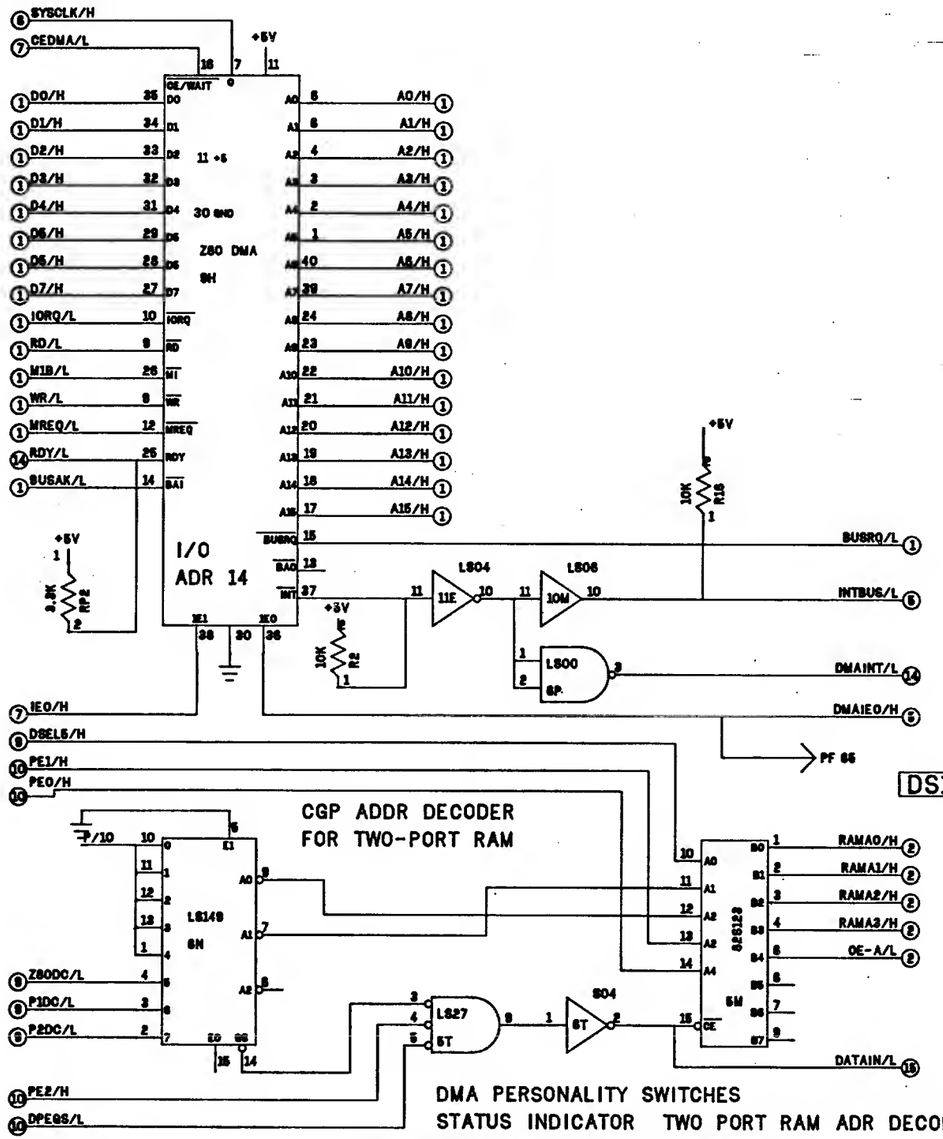
DA14E650 1

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

P.C.U.
SCHEMATIC DIAGRAM
DWG NO. DS14E652
SHT 4 OF 16 SHTS


7.3729 MHZ
OSC K1114A
LS74
LS367
LS00
LS21
LS04
LS11
LS375
LS148
INT LATCH
INT. PRIORITY ENCODER
INT LATCH
3PSWITCH
JP1
PUSH PULL DRIVER
2N3906
SYSCLK/H
INT/L
D0/H
D1/H
D2/H
D3/H
D4/H
D5/H
D6/H
D7/H
DATASETRDY0/H
DATASETRDY1/H
+12V
-12V
+12VM
-5VM
MRESET/H
LS132
ZRESET/L
RESTART
SWITCH
IORST/L
INTERRUPT VECTOR GENERATOR
DS14E652
SEE SHEET 1
P.C.U.
SCHEMATIC DIAGRAM
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
SHT 5 OF 16 SHTS





SEE SHEET 1

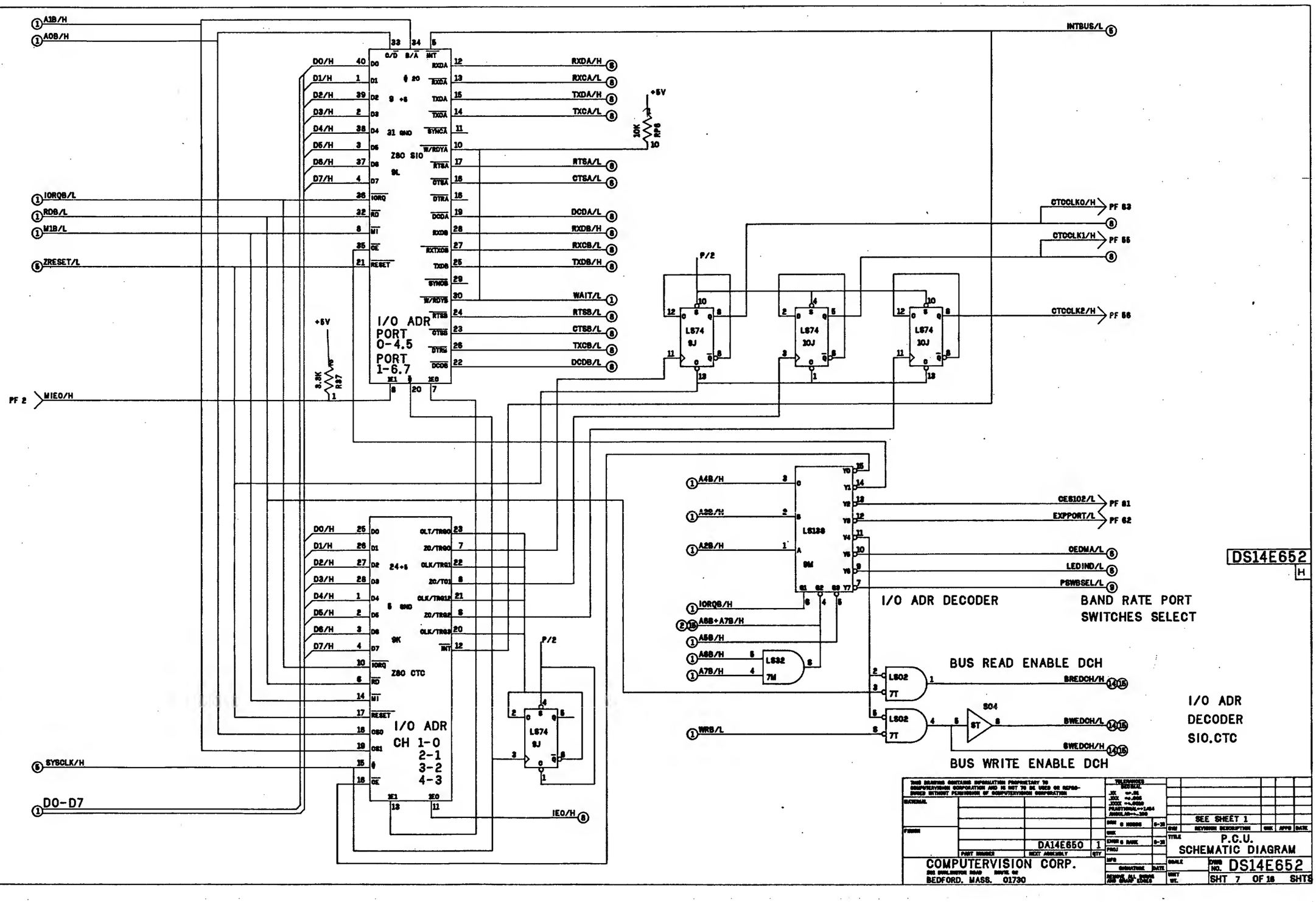
PART NUMBER	NEXT ASSEMBLY	QTY
DA14E650		1

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TITLE: P.C.U. SCHEMATIC DIAGRAM

DWG NO. DS14E652

SHT 6 OF 18 SHTS


A1B/H
A0B/H
INTBUS/L
D0/H
D1/H
D2/H
D3/H
D4/H
D5/H
D6/H
D7/H
Z80 SIO
9L
RXDA/H
RXCA/L
TXDA/H
TXCA/L
RTSA/L
CTSA/L
DCDA/L
RXDB/H
RXCB/L
TXDB/H
WAIT/L
RTSB/L
CTSB/L
TXCB/L
DCDB/L
+5V
10K
RP6
IORQB/L
RDB/L
M1B/L
ZRESET/L
I/O ADR
PORT
0-4.5
PORT
1-6.7
+5V
3.3K
R87
PF 2
MIEO/H
P/2
LS74
9J
LS74
10J
LS74
10J
CTCCLK0/H
PF 83
CTCCLK1/H
PF 85
CTCCLK2/H
PF 86
A4B/H
A3B/H
A2B/H
LS138
9M
CES102/L
EXPPORT/L
PF 81
PF 82
OEDMA/L
LEDIND/L
PSWBSEL/L
I/O ADR DECODER
BAND RATE PORT
SWITCHES SELECT
IORQB/H
A5B+A7B/H
A5B/H
A6B/H
A7B/H
LS32
7M
WRB/L
BUS READ ENABLE DCH
LS02
7T
LS02
7T
S04
BREDCH/H
BWEDCH/L
BWEDCH/H
BUS WRITE ENABLE DCH
I/O ADR
DECODER
SIO.CTC
DO/H
D1/H
D2/H
D3/H
D4/H
D5/H
D6/H
D7/H
Z80 CTC
9K
I/O ADR
CH 1-0
2-1
3-2
4-3
SYSCLK/H
DO-D7
IEO/H
DS14E652
H
SEE SHEET 1
P.C.U.
SCHEMATIC DIAGRAM
DS14E652
SHT 7 OF 16 SHTS
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
DA14E650

RXDA.DCDA

SIO PORT 0
LOOPBACK MUX
LOW SELECT
A INPUTS

OPEN=EIA
CLOSED=
CURRENT LOOP

OPEN=MODEM
CLOSED=LOCAL

TXDA.RTSA

OPEN=EIA
CLOSED=CURRENT LOOP

S10 PORT 1
LOOPBACK MUX

OPEN=MODEM
CLOSED=LOCAL

RXDB.DCDB

TXDB.RTSB
SIO PORT 1

OPEN=FORCED DTR
CLOSED=PROGRAMMABLE DTR

SIO PORT
LOOPBACK
CONTROL LATCH
I/O ADR 2C

SIO COMMUNICATIONS INTERFACE

DS14E652
H

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BEDFORD, MASS. 01730

DA14E650 1

SEE SHEET 1

P.C.U.
SCHEMATIC DIAGRAM

DWG NO. DS14E652

SHT 8 OF 16 SHTS

DEVICE SELECT PCU

CLOSE TO DISABLE PORT 0

CLOSE TO DISABLE PORT 1

DEVICE SELECT PORT 1

DEVICE CODE LOGIC Z80 BUSY/DONE

DS14E652

H

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BEDFORD, MASS. 01730

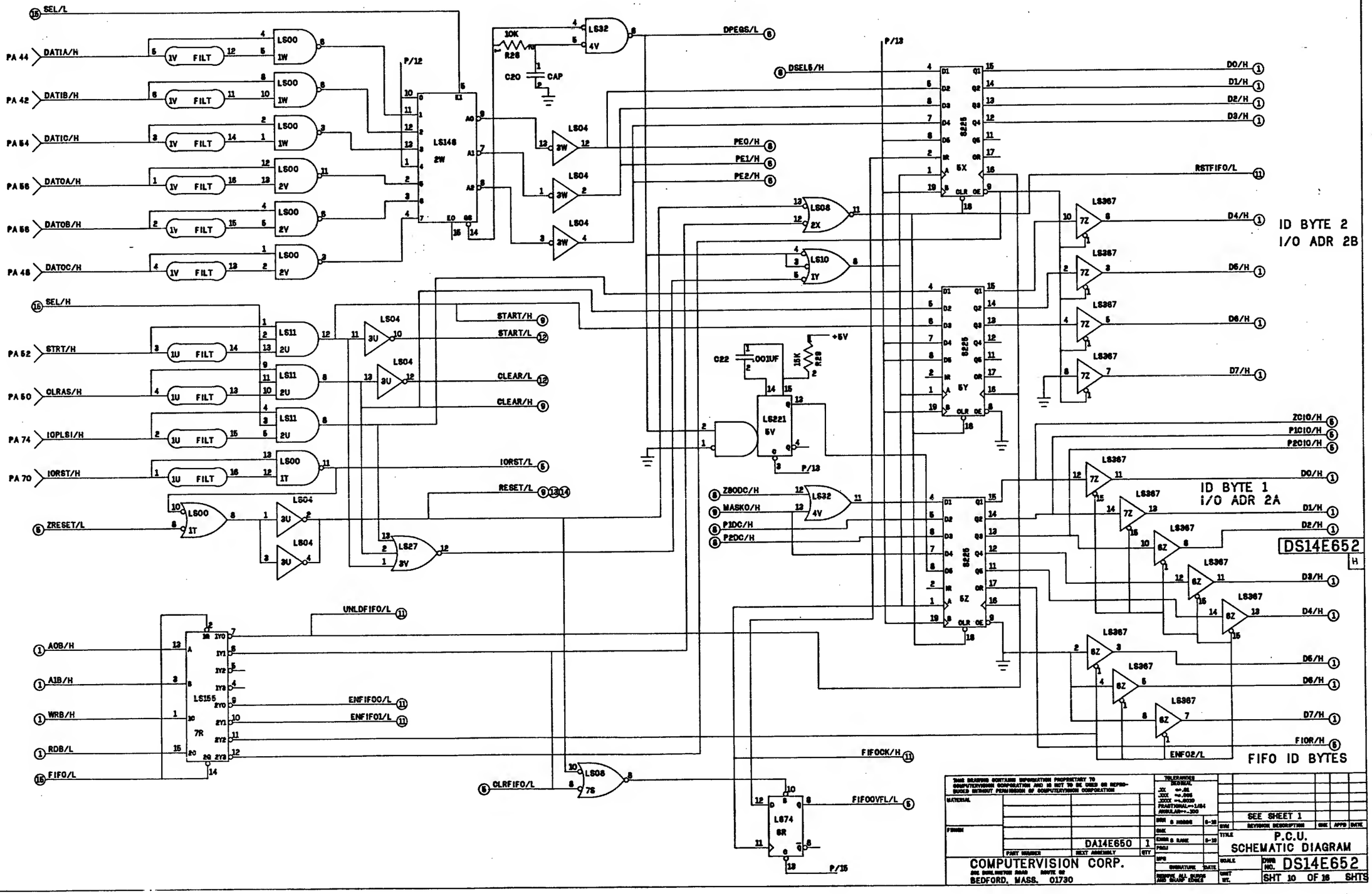
DA14E650 1

SEE SHEET 1

P.C.U. SCHEMATIC DIAGRAM

DWG NO. DS14E652

SHT 9 OF 16 SHTS


SEL/L
PA 44 DATIA/H
PA 42 DATIB/H
PA 54 DATIC/H
PA 56 DATOA/H
PA 58 DATOB/H
PA 48 DATOC/H
1V FILT
LS00 1W
LS00 2V
P/12
LS148 2W
10K R28
C20 CAP
LS32 4V
DPEGS/L
DSELS/H
PE0/H
PE1/H
PE2/H
LS04 3W
LS08 2X
LS10 1Y
SEL/H
PA 52 STRT/H
PA 50 CLRAS/H
PA 74 IOPLSI/H
PA 70 IORST/H
ZRESET/L
1U FILT
LS11 2U
LS00 1T
LS04 3U
LS27 3V
START/H
START/L
CLEAR/L
CLEAR/H
IORST/L
RESET/L
+5V
C22 .001UF
15K R29
LS221 5V
LS825 5X
LS825 5Y
LS825 5Z
RSTFIFO/L
D0/H
D1/H
D2/H
D3/H
D4/H
D5/H
D6/H
D7/H
LS367 7Z
LS367 6Z
ID BYTE 2
I/O ADR 2B
ID BYTE 1
I/O ADR 2A
Z80DC/H
MASKO/H
P1DC/H
P2DC/H
Z1O/H
P1IO/H
P2IO/H
DO/H
D1/H
D2/H
D3/H
D4/H
D5/H
D6/H
D7/H
FIOR/H
ENF02/L
A0B/H
A1B/H
WRB/H
RDB/L
FIFO/L
LS155 7R
UNLDFIFO/L
ENFIF00/L
ENFIF01/L
CLRFIFO/L
LS08 7S
FIFOCK/H
FIFOOVFL/L
LS74 8R
P/15
DS14E652
H
FIFO ID BYTES
SEE SHEET 1
P.C.U.
SCHEMATIC DIAGRAM
DA14E650
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
DWG NO. DS14E652
SHT 10 OF 16 SHTS

FIFO BYTE 1
I/O ADR 28
(LOW ORDER)

FIFO
BYTE 2
I/O ADR 29
(HIGH ORDER)

CGP TO BUS
TRANSCEIVERS

DCHI DATA REGISTERS

DATA FIFO DCH REGISTERS

DS14E652

REV H

SEE SHEET 1

REVISION DESCRIPTION	ENG	APPD	DATE

TITLE P.C.U.
SCHEMATIC DIAGRAM

DWG NO. DS14E652

SHT 11 OF 18 SHTS

DA14E650 1

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

DEVICE RESPONSE MUX

P1DS0/H
ZDS0/H
P2DS0/H
P/S
ZDS1/H
P1DS1/H
P2DS1/H
LS253 4G
LS367 6M
LS367 6M
ODATA8/H
ODATA9/H
ODATA10/H
ODATA11/H

P1DS2/H
ZDS2/H
P2DS2/H
ZDS3/H
P1DS3/H
P2DS3/H
LS253 3G
ODATA12/H
ODATA13/H

P1DS4/H
ZDS4/H
P2DS4/H
LS253 2G
ODATA14/H
ODATA15/H

PCUMSK/H

P/S
IRP20T/L
IRP10T/L
IRP2IN/L
IRP1IN/L
Z80INTR/L
LS148 1G
LS04 2S
LS04 2S
INT/L
PB 29

D0B/H
A0B/H
A1B/H
WRPRTBTS/H
WRPRTBTS/L
D1B/H
D2B/H
D3B/H
D4B/H
D5B/H
D6B/H
D7B/H
LS04 6N
LS04 6N
LS04 6N
LS04 7N
LS04 7N
LS04 7N
LS155 4N
LS155 3N
LS155 2N
LS155 1N
CP1IB/L
CP2IB/L
SP1ID/L
SP2ID/L
DP11INT/L
DP21INT/L
EP11INT/L
EP21INT/L
CP10B/L
CP20B/L
SP10D/L
SP20D/L
DP10INT/L
DP20INT/L
EP10INT/L
EP20INT/L

I/O FLAG CONTROL DECODER

P20DN/H
P10DN/H
P1IDN/H
P2IDN/H
P10BS/H
P20BS/H
P1IBS/H
P2IBS/H
DSEL9/L
P1DC/L
LS253 1R
7438 3R
7438 3R
SELD/L
SELB/L

PORT BUSY /
DONE SELECT

PA 98
INTPIN/L
PA 40
INTA/H
LS04 2S
LS04 2S
1V FILT
LS08 7S
LS11 4S
MINTA/L
MINTA/H

INT
PRIORITY

+5V
330 R24
7438 1S
INTPOUT/L
PA 96
330 R23

START/L
P2DC/H
DSEL5/H
PORTDC/H
PORTDC/L
CLEAR/L
LS155 2R
P11STRT/L
P21STRT/L
P10STRT/L
P20STRT/L
P11CLR/L
P21CLR/L
P10CLR/L
P20CLR/L

PORT BUSY/
DONE CONTROL

PORT 0.1-CGP INTERFACE

DS14E652
H

MATERIAL
FINISH
PART NUMBER DA14E650 1
NEXT ASSEMBLY QTY

TOLERANCES UNLESS
XX +-.01
XXX +-.005
XXXX +-.0020
FRACTIONAL +-1/64
ANGULAR +-.25°

DRN S HUGGS 6-29
CHK
ENGR S BANE 6-29
PROJ
APPD
SIGNATURE DATE

COMPUTERVISION CORP.
300 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

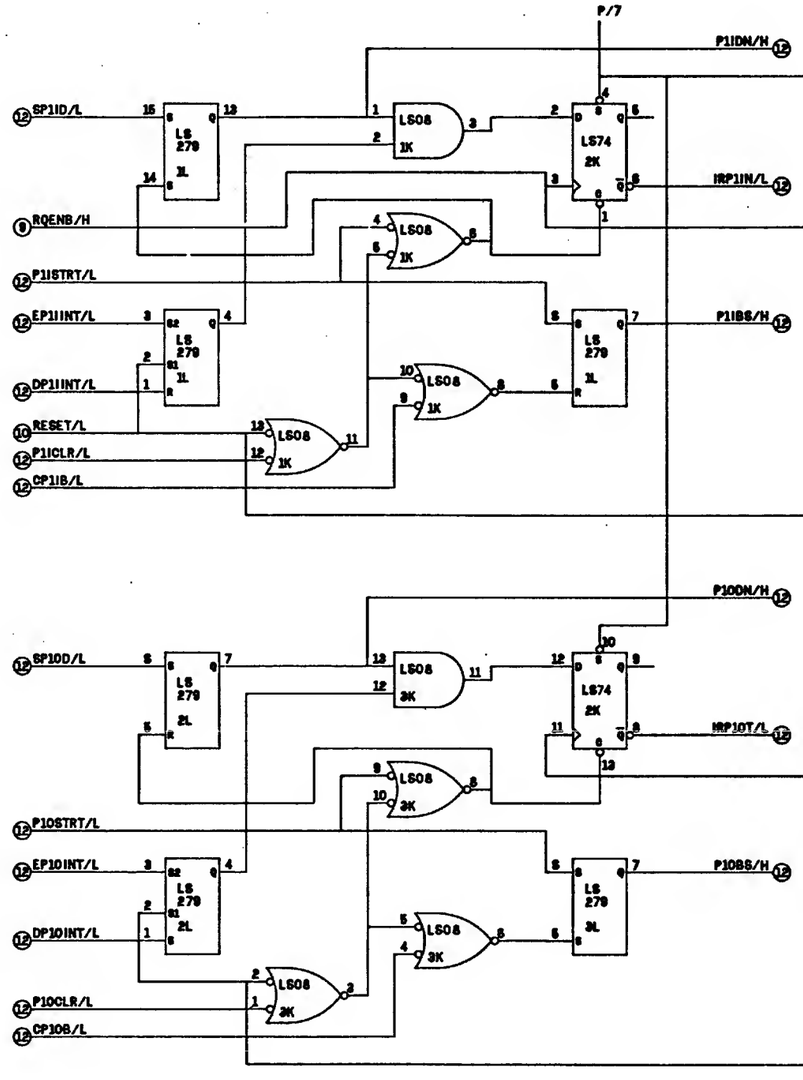
SEE SHEET 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE P.C.U.
SCHEMATIC DIAGRAM

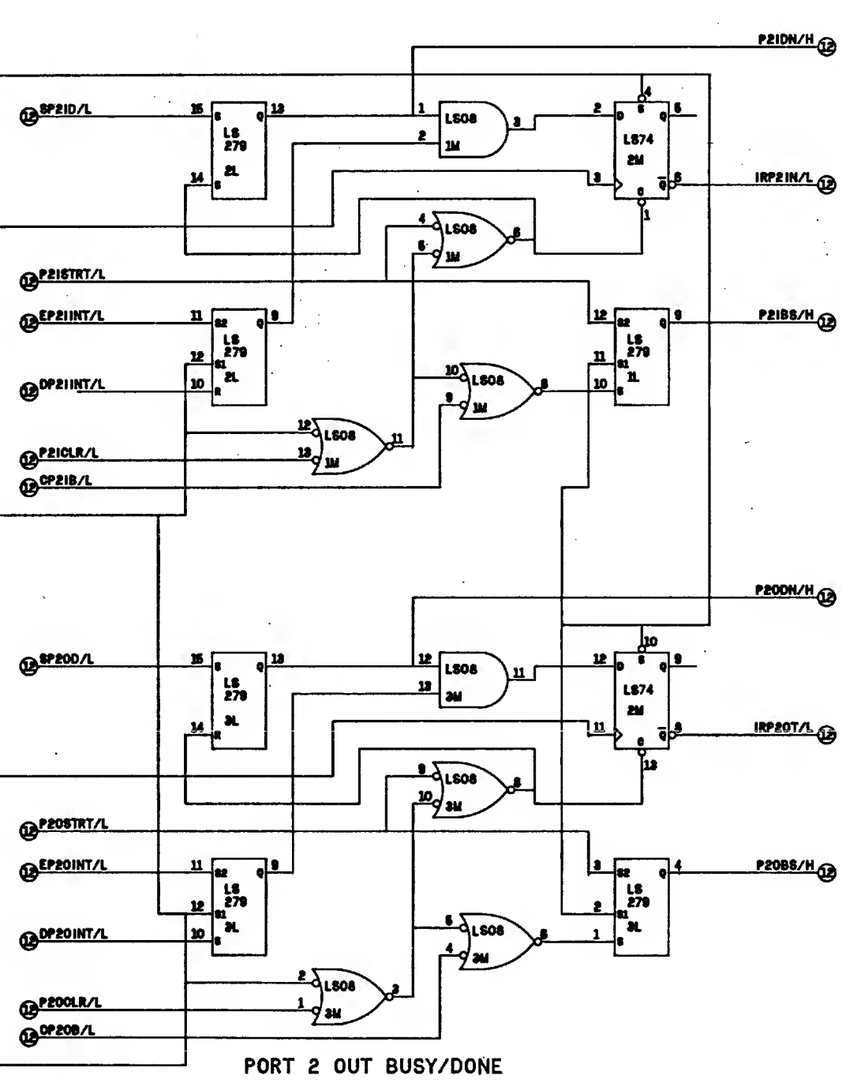
SCALE
DWG NO. DS14E652
SHT SIZE
SHT 12 OF 18 SHTS

PORT 0 IN BUSY/DONE



PORT 0 OUT BUSY/DONE

PORT 1 IN BUSY/DONE



PORT 2 OUT BUSY/DONE

PORT 0-1 BUSY/DONE

DS14E652
H

MATERIAL	PART NUMBER	NEXT ASSEMBLY	QTY
FINISH	DA14E650		1

TOLERANCES UNLESS OTHERWISE SPECIFIED: DECIMAL .XX ±.01, .XXX ±.005, .XXXX ±.0050, FRACTIONAL ±1/64, ANGULAR ±.30°

	SIGNATURE	DATE
DRAWN		
MFG		

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

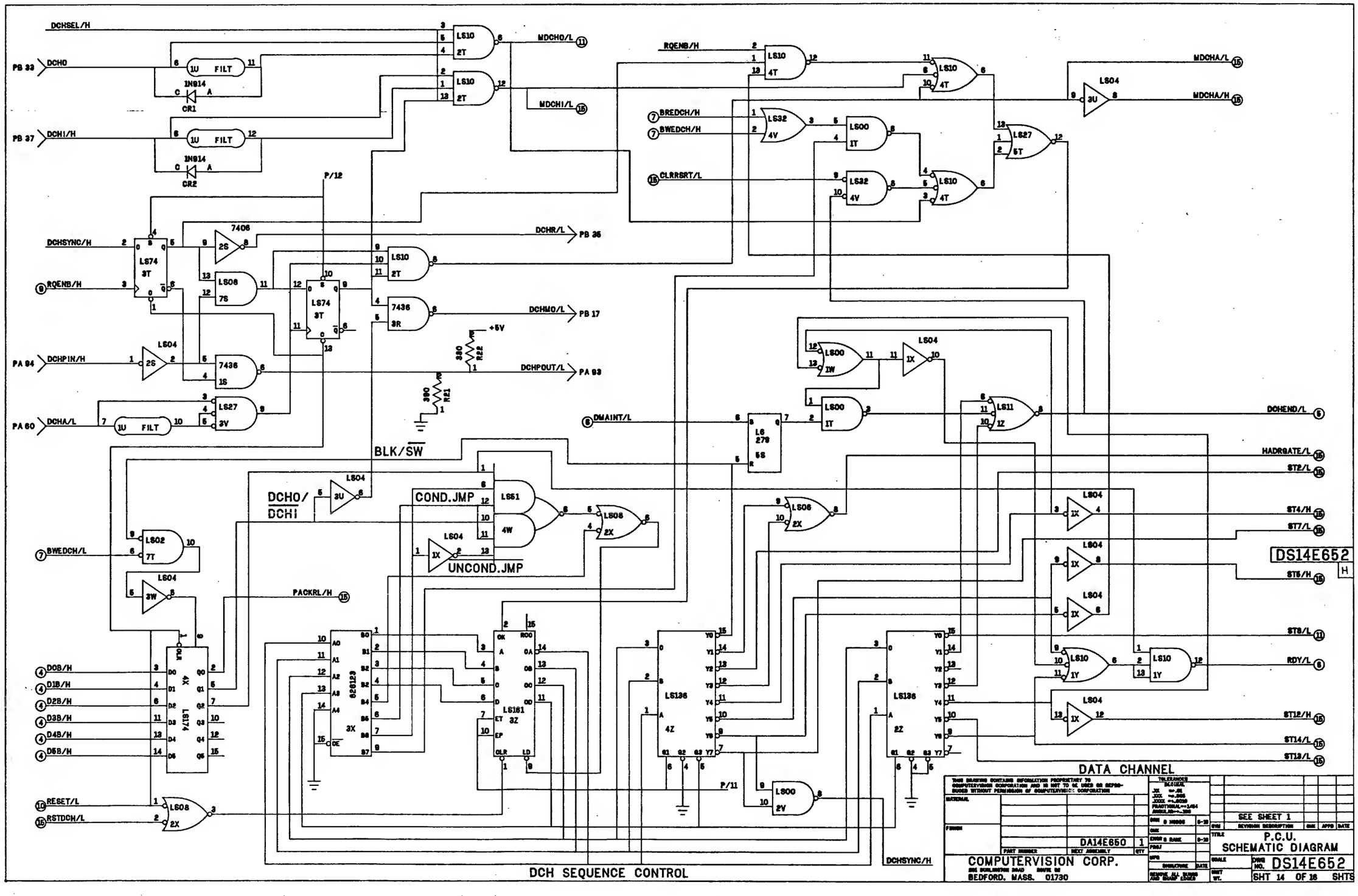
SEE SHEET 1

DWG	REVISION DESCRIPTION	ENG	APPD	DATE

TITLE: P.C.U. SCHEMATIC DIAGRAM

SIZE: C | DWG NO. DS14E652

SHT 12 OF 16 SHTS


DCHSEL/H
PB 33 DCH0
PB 37 DCH1/H
1U FILT
1N914
CR1
CR2
LS10
MDCH0/L
MDCH1/L
P/12
DCHSYNC/H
RQENB/H
LS74
3T
7406
2S
LS08
7S
DCHR/L
PB 35
7436
3R
DCHM0/L
PB 17
+5V
390 R22
DCHPOUT/L
PA 93
PA 94 DCHPIN/H
LS04
7436
1S
PA 80 DCHA/L
LS27
3V
390 R21
BLK/SW
DCH0/
DCH1
COND.JMP
LS51
4W
LS08
2X
UNCOND.JMP
LS04
7 BWEDCH/L
LS02
7T
3W
PACKRL/H
4 DOB/H
4 D1B/H
4 D2B/H
4 D3B/H
4 D4B/H
4 D5B/H
LS174
4X
82S123
3X
LS161
3Z
10 RESET/L
15 RSTDCH/L
LS08
2X
RQENB/H
LS10
4T
7 BREDCH/H
7 BWEDCH/H
LS32
4V
LS00
1T
15 CLRRSRT/L
LS32
4V
LS10
4T
LS27
5T
LS04
3U
MDCHA/L
MDCHA/H
8 DMAINT/L
L6
278
5S
LS00
1W
LS04
1X
LS00
1T
LS11
DCHEND/L
HADRGATE/L
ST2/L
ST4/H
ST7/L
DS14E652
H
ST5/H
LS04
1X
LS04
1X
LS10
1Y
LS10
1Y
ST8/L
RDY/L
LS04
1X
ST12/H
ST14/L
ST13/L
LS06
2X
LS00
2V
P/11
LS136
4Z
LS136
2Z
DCHSYNC/H
DATA CHANNEL
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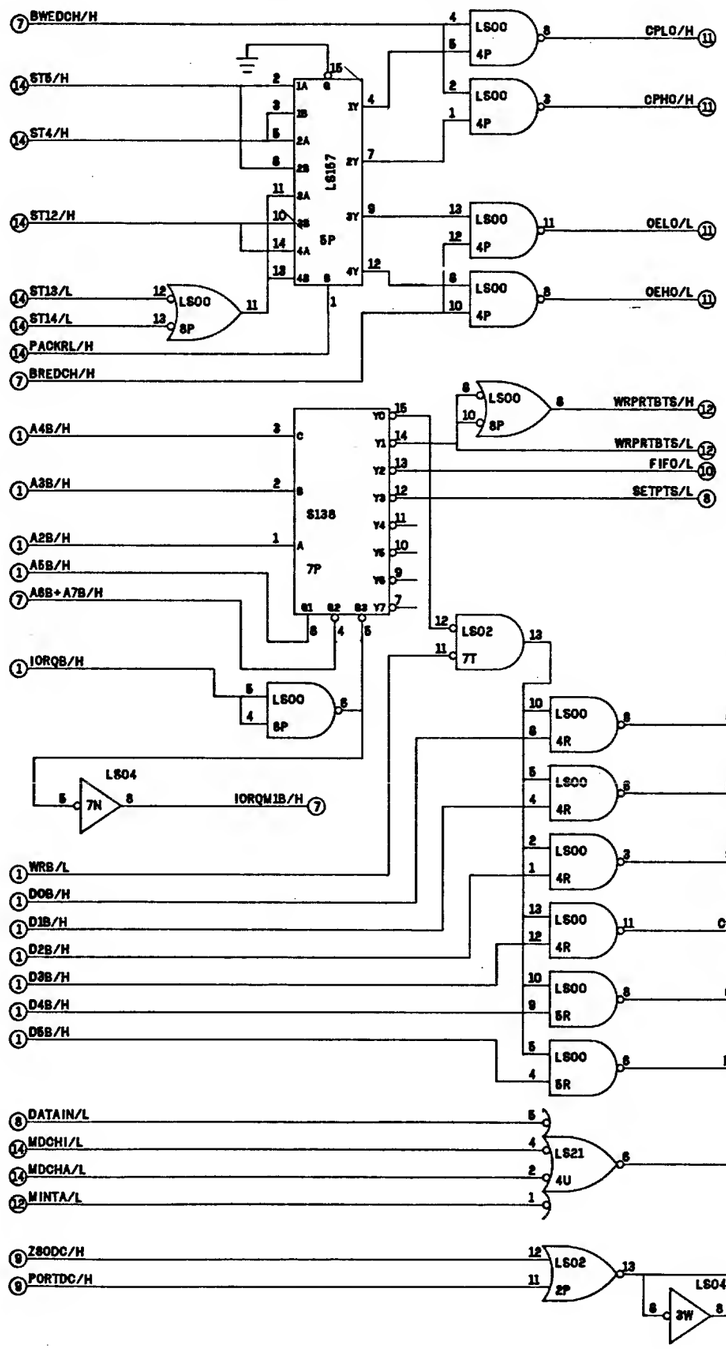
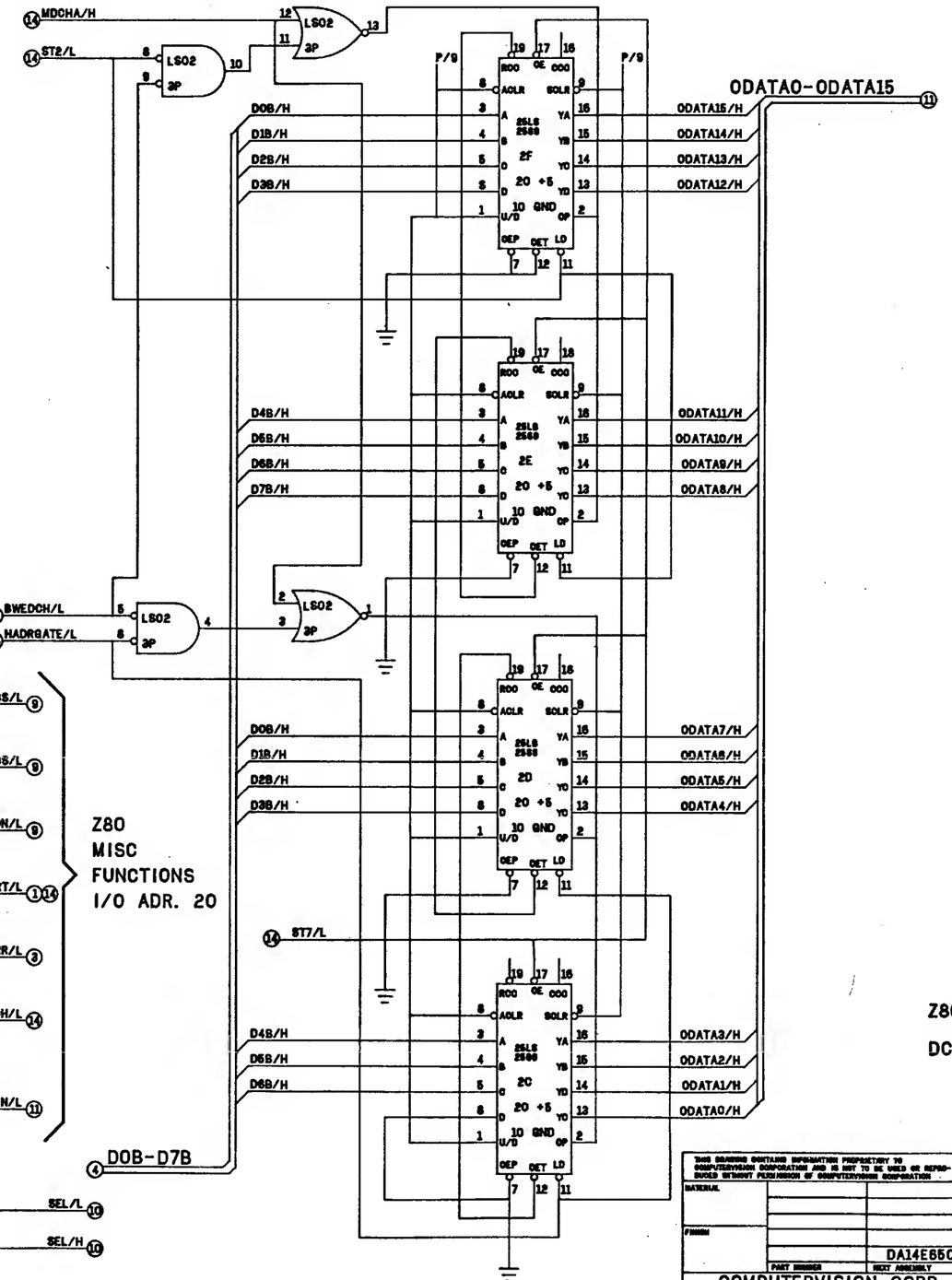
MATERIAL
FINISH
PART NUMBER DA14E650 1
NEXT ASSEMBLY QTY
TOLERANCES
DECIMAL
.XX +-.05
.XXX +-.005
.XXXX +-.0050
FRACTIONAL +-1/64
ANGULAR +-.25°
DRN
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES
SEE SHEET 1
REVISION DESCRIPTION CHK APPD DATE
TITLE P.C.U.
SCHEMATIC DIAGRAM
SCALE
DWG NO. DS14E652
SHT WT.
SHT 14 OF 16 SHTS
COMPUTERVISION CORP.
300 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730
DCH SEQUENCE CONTROL

BYTE PACKING DIREOTION CONTROL



Z80
MISC
FUNCTIONS
I/O ADR. 20



DS14E652
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Z80 MISC FUNCTIONS
DCH ADDER COUNTER

PART NUMBER	NEXT ASSEMBLY	QTY
DA14E650		1

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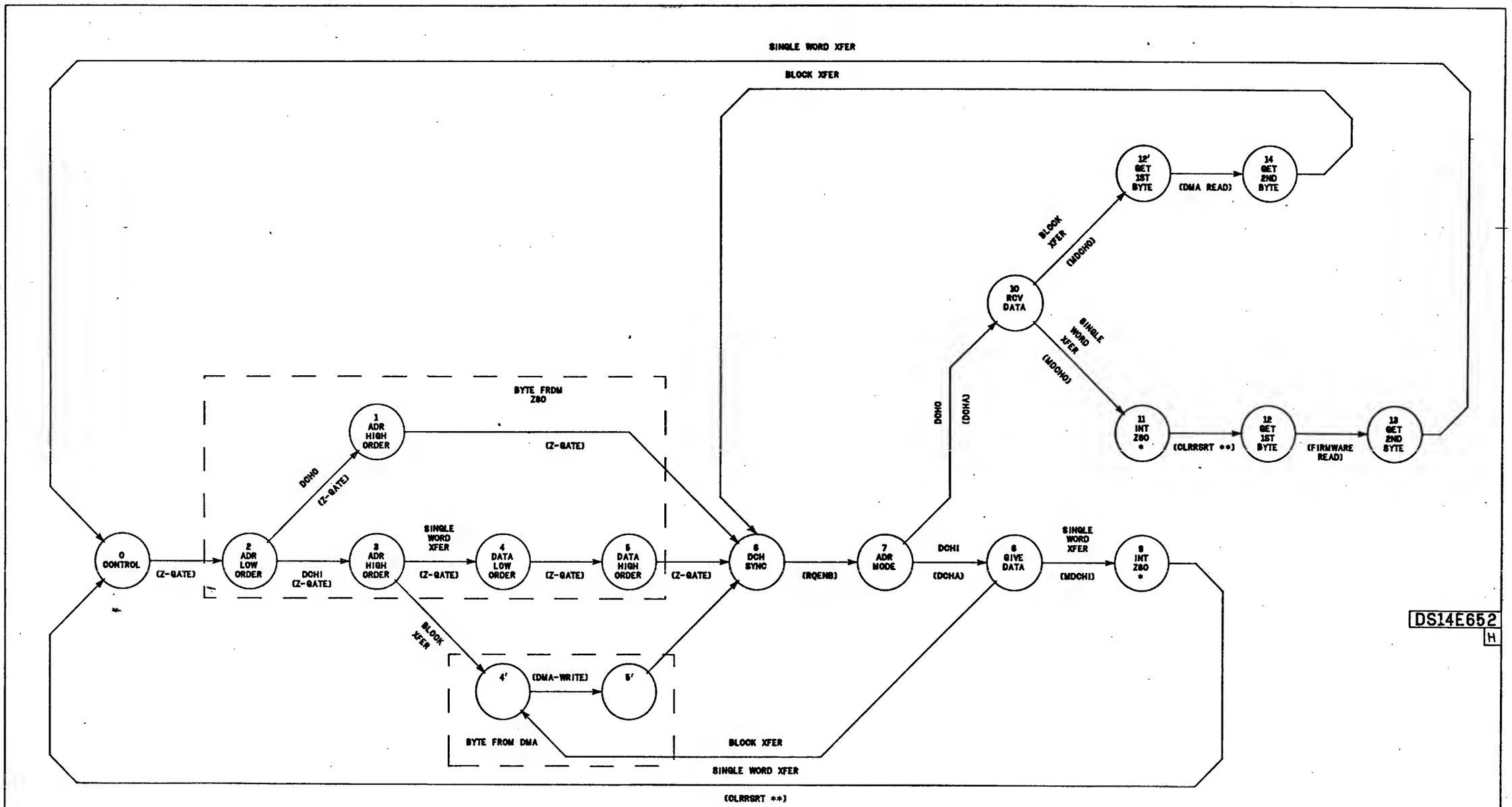
TITLE: P.C.U.
SCHEMATIC DIAGRAM

DWG NO. DS14E652

SHT 15 OF 16 SHTS



DS14E652
H

* DCHEND INT

** CLEARS DCH INT

SIGNALS IN PARENTHESES CAUSE THE STATES TO ADVANCE.

DATA CHANNEL CONTROLLER STATE DIAGRAM

MATERIAL		
FINISH	DA14E650	1
	PART NUMBER	QTY

TOLERANCES UNLESS DIMENSIONAL .XX +-.01 .XXX +-.005 .XXXX +-.0050 FRACTIONAL +-1/64 ANGULAR +-.30

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

TITLE: P.C.U. SCHEMATIC DIAGRAM

DWG NO. DS14E652

SHT 16 OF 16 SHTS

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